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UNITED STATES

SECURITIES AND EXCHANGE COMMISSION
WASHINGTON, DC 20549

FORM SE

FORM FOR SUMISSION OF PAPER FORMAT EXHIBITS
BY ELECTRONIC FILERS

Ramtron International Corporation	0000849502
Exact Name of Registrant as Specified in Charter	Registrant CIK Number
Form 10-Q For June 30, 2003	000-17739
Electronic Report, Schedule or Registration Statement of Which the Documents Are a Part (give period of report)	SEC File Number, if available

Name of Person Filing the Document
(If Other than the Registrant)

SIGNATURES

The Registrant has duly cause this form to be signed on its behalf by the undersigned, thereunto duly authorized, in the City of Colorado Springs, State of Colorado, August 19, 2003.

RAMTRON INTERNATIONAL CORPORATION
(Registrant)

LuAnn D. Hanson
Chief Financial Officer

IN ACCORDANCE WITH RULE 202 OF REGULATION S-T, THIS EXHIBIT 10.1* TO FORM 10-Q (JUNE 30, 2003) IS BEING FILED IN PAPER PURSUANT TO A CONTINUING HARDSHIP EXEMPTION.

AMENDMENT NUMBER TWO TO HP/EMS MANUFACTURING AGREEMENT

This AMENDMENT NUMBER TWO TO HP/EMS MANUFACTURING AGREEMENT (the "AMENDMENT") is entered into as of April 14, 2003 ("Amendment Effective Date") by and among Enhanced Memory Systems, a Delaware corporation ("EMS"), Ramtron International Corporation, a Delaware corporation ("RIC") and Hewlett-Packard Company, a Delaware corporation ("HP").

WHEREAS, HP and EMS entered into a the "HP/EMS Manufacturing Agreement" effective May 26, 2000, as amended by the "Amendment to HP/EMS Manufacturing Agreement" dated February 8, 2002 (collectively, the "Manufacturing Agreement") for the design of an HP Product generally described as an Embedded-DRAM for manufacture in Infineon's 0.17 um Embedded-DRAM process (the design and development of the HP Product is also referred to as the "Pegasus Project");

WHEREAS, RIC is the owner of EMS and, as such, will be a party to the Manufacturing Agreement;

WHEREAS, HP, RIC and EMS wish to further amend the Manufacturing Agreement to provide for (a) the immediate transfer of title and possession rights of certain Necessary Software and Hardware from EMS and RIC to HP, (b) the provision by EMS and RIC to HP of use of, and access to, certain supply chain equipment and vendors, (c) the provision by EMS and RIC to HP of contract engineering services for design, development and product support, (d) a restatement of the current Statement of Work.

NOW THEREFORE, HP, RIC and EMS agree to amend the Manufacturing Agreement as follows:

1. RIC is hereby made a party to the Manufacturing Agreement. Accordingly, HP, EMS and RIC hereby agree that wherever the term "EMS" appears in the Manufacturing Agreement, the term "EMS" shall be understood to mean Enhanced Memory Systems, a Delaware corporation ("EMS") and Ramtron International Corporation, a Delaware corporation ("RIC").

2. The following Sections will be added to Section 2 ("Definitions") of the Manufacturing Agreement:

   2.23 "Direct Personnel Cost" shall mean EMS or RIC actual payroll costs for personnel (including HP directed travel) and burdened administrative overhead (general management, finance, human resources, account services, and administrative support).

   2.24 "Key Personnel" shall mean the EMS and RIC personnel specified in Exhibit P-2 annexed hereto that are considered to be essential to the work being performed under this Agreement.

   2.25 "WIP" shall mean material work in process to support HP purchase orders and development and debug requirements.

3. Delete Section 4.2.5 of the Manufacturing Agreement in its entirety and replace with the following:

   4.2.5 Notwithstanding anything to the contrary in the Agreement and subject to the limits of any licenses or confidentiality agreements with third parties, EMS hereby grants to HP, under EMS' Intellectual Property Rights, a transferable, worldwide, royalty-free, perpetual, irrevocable, and paid-up license to make, have made, use, sell, and have sold the HP Product, and all future derivatives and follow-ons of the HP Product as determined by HP, for HP's use and sale in HP and/or ** manufactured systems incorporating such HP Product including, but not limited to, HP OEM daughter cards.

   (i) In addition, EMS also hereby grants to HP as of the Amendment Effective Date, under EMS' Intellectual Property Rights, a worldwide, royalty-free, perpetual, irrevocable, and paid-up right to sublicense the rights granted to HP in Section 4.2.5, above, to ** to

future derivatives and follow-ons of the HP Product as determined by HP) including, but not limited to, HP OEM daughter cards; provided, however, that HP shall not grant such sublicense rights to ** unless and until HP first terminates this Agreement in accordance with Section 23.5, below.

This Section 4.2.5 shall survive termination or expiration of this Agreement.

4. Delete Section 4.6 of the Manufacturing Agreement in its entirety and replace with the following:

4.6 Upon execution of this Amendment, EMS and RIC shall immediately transfer title and physical possession to HP of the Necessary Software and Hardware set forth in Exhibit N-2. If transfer cannot be effected then: (i) such Necessary Software and Hardware shall be tagged as HP Property solely for the purposes of Sections 4.2.5 and 23.2; (ii) EMS appoints HP as its attorney-in-fact for the sole purpose of executing and filing, on EMS's and RIC's behalf, UCC-1 financing statements (and any appropriate amendments thereto), as required by HP for protective purposes to evidence HP's continuing right, title and ownership of the Necessary Software and Hardware; and, (iii) HP may, from time to time, inspect the Necessary Software and Hardware. HP hereby grants back to EMS and RIC, a paid-up, royalty-free license to make, use and sell EMS products using such Necessary Software and Hardware for any EMS or RIC product.

5. Delete Section 23.5 of the Manufacturing Agreement in its entirety and replace with the following:

23.5 HP Termination. If HP terminates this Agreement or an Exhibit hereto due to EMS's and/or RIC's breach under this Section 23, (a) EMS and RIC shall not be obligated to accept further applicable purchase orders after receiving notice and (b) HP may cancel any previously accepted purchase orders, and (c) HP shall be entitled to exercise the rights set forth in Section 4.2.5(i). In addition, HP may procure, upon such terms and in such manner as HP reasonably deems appropriate, products similar to the HP Product as to which this Agreement or an Exhibit is terminated. EMS and RIC agree to reimburse HP upon demand for additional costs incurred by HP in purchasing, qualifying and testing such products that are similar to the HP Products. In no event, shall EMS or RIC pay mutually agreed upon NRE costs in excess of those NRE payments made to EMS and RIC by HP under this Agreement. EMS and RIC further agree to continue the performance of this Agreement to the extent not terminated under the provisions of this Section.

EMS and RIC also agree to provide all Deliverables, in their then current state, as defined in Section 23.6 below and provide continuing IP rights to HP as further defined in this Agreement.

Notwithstanding anything to the contrary contained in this Section 23.5, the parties agree that any EMS or RIC failure to meet either (a) the ITY and packaging goals set forth in Section 4.1.7 of Exhibit F-2 ("Product yield"), or (b) the production wafer test and production final packaged part test times set forth in Section 4.1.8 of Exhibit F-2 ("Test time") shall not be deemed an event of breach that will trigger EMS' and RIC's obligation to reimburse HP for additional costs incurred by HP in purchasing, qualifying and testing of products that are similar to the HP Products.

6. Delete Section 23.7 of the Manufacturing Agreement in its entirety and replace with the following:

23.7 EMS and RIC agree that HP may immediately send copies of the letter agreement set forth in Exhibit O to EMS' suppliers . EMS and RIC further agree to support HP's direct negotiations with such EMS and/or RICs to provide assurances of the supply of HP Product.

7. EMS and RIC shall maintain current levels of resources for the Pegasus Project through the duration of activities set forth in Exhibit F-2 ("Statement of Work) annexed hereto. Ongoing product engineering support includes, but is not limited to, test program and development support, Burn In vectors

development, and support, qualification and process flows. EMS and RIC shall provide HP with engineering and development services, as requested by HP, through the completion of the Statement of Work set forth in Exhibit F-2 attached hereto. Upon HP's request and to the extent that the EMS and RIC personnel listed in Exhibit P-2 are still employed by EMS and/or RIC, EMS and RIC shall provide additional design, development and/or sustaining engineering services in accordance with the fees set forth in Section 11 , below, or as otherwise agreed to by the parties.

8. EMS and RIC shall exercise best efforts to keep Key Personnel assigned to the Pegasus Project. Any changes to Key Personnel must be approved in advance by HP, which permission shall not be unreasonably withheld. Any reassignment, transfer, or removal of Key Personnel shall be limited to the following: (a) voluntary resignation, (b) transfer based on personal choice, (c) reassignment for promotional reasons, (d) termination for cause in accordance with EMS or RIC policies, (e) extenuating personal circumstances, and/or (f) mutual agreement. In the event that any of the Key Personnel will be or are unavailable for extended periods for the regular performance of their duties, EMS and/or RIC will designate and propose to HP, subject to HP prior approval, an equally qualified alternate. Upon mutual agreement, the parties may add and/or delete Key Personnel to Exhibit P-2.

9. Notwithstanding anything to the contrary contained in the Manufacturing Agreement or this Amendment and upon assumption by HP of all costs and invoices for HP-designated pre-fuse WIP, EMS and RIC shall immediately provide HP with title and possession of such materials. No later than thirty (30) days after the Amendment Effective Date, HP shall provide Purchase Order(s) to Infineon for such pre-fuse WIP.

10. HP shall not be obligated to make any further payments to EMS or RIC regarding, and shall in no event be liable for, any expenses or liabilities incurred by EMS or RIC prior to the Amendment Effective Date including, but not limited to, EMS' or RIC's acquisition of masks, design db, or any other items set forth in Exhibit N-2. Notwithstanding anything to the contrary in this Section 10., HP shall pay the applicable third parties (and not EMS or RIC) for acquisition of masks that follow EMS' or RIC's A4 revision.

11. HP shall pay for EMS and RIC contract engineering services and ongoing product support services provided to HP after the Amendment Effective Date at a rate equal to EMS' or RIC's Direct Personnel Cost, as applicable. HP shall provide EMS and/or RIC, as applicable, with an Order requesting any such EMS or RIC services. The parties agree that the anticipated Direct Personnel Costs of EMS or RIC, as applicable, through completion of the Statement of Work as set forth in Exhibit F-2 attached hereto shall not exceed One Million Five Hundred Thousand ($1,500,000) Dollars without HP's prior written authorization to EMS and RIC to enable EMS and RIC to exceed such estimated costs. Exhibit S attached hereto identifies the operational terms and conditions for the ordering and payment of contract engineering services to be provided by EMS and RIC under the Manufacturing Agreement.

12. Commencing upon the Amendment Effective Date, HP shall pay EMS and RIC for HP's use of tester equipment located in Colorado Springs at the monthly rate of Sixty-four Thousand ($64,000) Dollars per month through October 1, 2003. EMS and RIC guarantee that HP shall have no less than six and one-half (6.5) hours of available test time per day between the hours of 6:00 AM through 9:00 PM, Monday through Friday. Test times outside the aforementioned timeframe shall be mutually agreed to. After October 1, 2003, HP, RIC and EMS will negotiate in good faith the parameters and fees for continued HP access to tester equipment and provision of test time support by EMS and RIC.

13. Should HP determine, in its sole discretion, that EMS and/or RIC efforts in helping HP meet each of HP's requirements (the "HP Acceptance Criteria") on or before certain specified dates, then HP agrees to pay EMS and/or RIC, as applicable and in addition to HP's payment of Direct Personnel Costs, a sum (an "Earned Incentive Fee") to be determined in accordance with this Section 12.

13.1. For the purposes of this Section 13, "HP Acceptance Criteria" shall mean:

i. Integrated Test Yield ("ITY") of forty (40%) percent or better;

ii. Escape rate of 5000PPM;

iii. Wafer test time of 100 sec;

iv. Package test time of 800 seconds (16 parts per DUT); and

13.2. Should EMS and/or RIC, as applicable meet each of the HP Acceptance Criteria on or before November 30, 2003, then EMS and/or RIC shall be entitled to receive from HP an Earned Incentive Fee equal to twenty (20%) percent of the Direct Personnel Costs billed to HP during the period commencing on the Amendment Effective Date through the date HP determines that EMS and/or RIC, as applicable, has met all of the HP Acceptance Criteria.

13.3. Should EMS and/or RIC, as applicable, meet each of the HP Acceptance Criteria on or before December 31, 2003, then EMS and/or RIC shall be entitled to receive from HP an Earned Incentive Fee equal to fifteen (15%) percent of the Direct Personnel Costs billed to HP during the period commencing on the Amendment Effective Date through the date HP determines that EMS and/or RIC, as applicable, has met all of the HP Acceptance Criteria.

13.4. Should EMS and/or RIC, as applicable, meet each of the HP Acceptance Criteria on or before January 31, 2004, then EMS and/or RIC shall be entitled to receive from HP an Earned Incentive Fee equal to ten (10%) percent of the Direct Personnel Costs billed to HP during the period commencing on the Amendment Effective Date through the date HP determines that EMS and/or RIC, as applicable, has met all of the HP Acceptance Criteria.

13.5. Should EMS and/or RIC, as applicable, meet each of the HP Acceptance Criteria on or before February 28, 2004, then EMS and/or RIC shall be entitled to receive from HP an Earned Incentive Fee equal to five (5%) percent of the Direct Personnel Costs billed to HP during the period commencing on the Amendment Effective Date through the date HP determines that EMS and/or RIC, as applicable, has met all of the HP Acceptance Criteria.

14. Should EMS' and/or RIC, as applicable, work product meet all HP-defined standards (the "HP Performance Standards") and be accepted by HP in accordance with such HP Performance Standards on or before certain specified dates, then HP agrees to pay EMS and/or RIC, as applicable and in addition to HP's payment of Direct Personnel Costs and any Earned Incentive Fee payments, a sum (an "Earned Performance Payment") to be determined in accordance with this Section 13.

14.1. For the purposes of this Section 14, "HP Performance Standards" shall mean:

v. ITY of seventy-five (75%) percent or better;

vi. Escape rate of 500 DPM;

vii. Wafer test time of 35 sec/part;

viii. Package test time of 320 seconds (16 parts per DUT); and

14.2. Should EMS and/or RIC, as applicable, meet each of the HP Performance Standards on or before the earlier occurrence of either (a) the six (6) month anniversary date of EMS' and/or RIC's attaining each of the HP Acceptance Criteria described in Section 13, above, or (b) July 1, 2004, then EMS and/or RIC shall be entitled to receive from HP an Earned Performance Payment equal to twenty (20%) percent of the Direct Personnel Costs billed to HP during the period commencing on the Amendment Effective Date through the date HP determines that EMS and/or RIC, as applicable, has met all of the Earned Performance Payment.

14.3. Should EMS and/or RIC, as applicable, meet each of the HP Performance Standards on or before the earlier occurrence of either (a) the seven (7) month anniversary date of EMS' and/or RIC's attaining each of the HP Acceptance Criteria described in Section 13, above, or (b) August 1,

2004, then EMS and/or RIC shall be entitled to receive from HP an Earned Performance Payment equal to fifteen (15%) percent of the Direct Personnel Costs billed to HP during the period commencing on the Amendment Effective Date through the date HP determines that EMS and/or RIC, as applicable, has met all of the Earned Performance Payment.

14.4. Should EMS and/or RIC, as applicable, meet each of the HP Performance Standards on or before the earlier occurrence of either (a) the eight (8) month anniversary date of EMS' and/or RIC 's attaining each of the HP Acceptance Criteria described in Section 13, above, or (b) September 1, 2004, then EMS and/or RIC shall be entitled to receive from HP an Earned Performance Payment equal to ten (10%) percent of the Direct Personnel Costs billed to HP during the period commencing on the Amendment Effective Date through the date HP determines that EMS and/or RIC, as applicable, has met all of the Earned Performance Payment.

15. Exhibit D of the Manufacturing Agreement is hereby deleted in its entirety.

16. Delete Exhibit F in its entirety and replace with Exhibit F-2 attached hereto.

17. Delete Exhibits H, I, and J in their entirety.

18. Delete Exhibit N in its entirety and replace with Exhibit N-2 attached hereto.

19. EMS shall provide HP with the rights to the equipment and materials as set forth in Exhibit Q-2 attached hereto. To enable HP to fully enjoy such rights, the parties hereby agree that should any EMS and/or RIC subcontractor refuse to disclose to HP any confidential information of EMS and/or RIC that is relevant to the activities, assets, or other contractual rights transferred from EMS and/or RIC to HP under the Manufacturing Agreement and/or this Amendment, then HP shall notify EMS and/or RIC, as applicable, of such inability to obtain such needed information. Upon receipt of HP's notice, EMS and/or RIC shall immediately inform such subcontractor that EMS and/or RIC agree to permit the subcontractor to disclose such EMS and/or RIC confidential information to HP.

20. Settlement and Release

20.1. Concurrent with the execution of this Amendment and except as set forth in this Amendment, each party, on behalf of itself and on behalf of each of its parent corporations, divisions, subsidiaries, affiliates, predecessors, successors, and assigns, hereby releases and forever discharges the other party, and each of said other party's respective parent corporations, divisions, subsidiaries, affiliates, predecessors, successors, assigns, officers, directors, trustees, heirs, beneficiaries, executors, administrators, attorneys, employees, and agents from any and all actions, causes of action, claims, counterclaims, cross claims, third party claims, debts, demands, liabilities, lawsuits, accounts, covenants, contracts, promises, agreements, doings, omissions, obligations, costs, attorneys' fees, expenses, damages, and claims of every name and nature, known and unknown, in law and in equity, which existed, may have existed and/or which could have been asserted from the beginning of the world to this date arising out of and/or relating to the Manufacturing Agreement, as amended, under any foreign, federal, state, or municipal law, regulation or common law cause of action.

20.2. Each party hereby waives and relinquishes any right or benefit which it has or may have against the other party as of the date of this Amendment concerning, arising out of, and/or relating to the Manufacturing Agreement regardless of whether said right or benefit was known or unknown at the time that the party executed this Amendment. In connection with such waiver and relinquishment, each party acknowledges that it is aware that it or its attorneys, agents, consultants, officers, employees, or accountants may hereafter discover claims or facts in addition to or different from those now known or believed to exist. Nevertheless, it is the intention of each party to fully, finally and forever settle, release, and agree not to sue over any and all such claims, causes of action, and other matters as set forth in this Amendment. In furtherance of this intention, the releases and agreements not to sue set forth in this Amendment shall be and remain

in effect as full and complete releases notwithstanding the subsequent discovery or existence of any such additional or different claim or fact.

In entering into this settlement and granting the releases and covenants not to sue set forth in this Amendment, each party knowingly and willingly waive any rights it may have under Section 1542 of the California Civil Code (and/or under any similar statute or law of any other jurisdiction), which provides:

> **Section 1542. A general release does not extend to claims which the creditor does not know or suspect to exist in his favor at the time of executing the release, which if known by him must have materially affected his settlement with the debtor.**

Each party also waives any right it may have under any similar federal law or statute and under any similar law or statute of another state or jurisdiction.

20.3. Each Party acknowledges it will not institute, maintain, assist or otherwise encourage any action, litigation or proceedings of any kind against the other nor aid any third party in any action against the other arising out of the Manufacturing Agreement.

20.4. The Parties agree that this Amendment may not be used as evidence in a proceeding of any kind except one in which a party alleges a breach of the terms of this Amendment or one in which a party elects to use this Amendment as a defense to any claim. In the event of breach of the terms of this Amendment, the breaching Party will indemnify and hold the other harmless from any claims resulting solely and directly from such breach of this Amendment including, but not limited to, attorney fees and costs.

20.5. Each Party disclaims any liability to the other, and it is expressly understood and agreed that neither this Amendment nor any actions referenced or required by this Amendment will be deemed evidence or an admission of any liability or wrongdoing by either party.

[Intentionally left blank]

20.6. Each Party represents and acknowledges this Amendment has been freely and voluntarily entered into and that no oral or written representations, statements, covenants, inducements warranties, or promises of any kind, unless specifically contained in this Amendment, have been made by either party to induce or otherwise influence the other to enter into this Amendment. Each of the Parties acknowledge that: they have been represented by counsel of their choice throughout the negotiation of this Amendment; their respective counsel has fully explained to them the legal effect of this Amendment and of the stipulation of dismissal with prejudice, the release, the covenant not to sue, and all other material provisions hereof; they are entering into this Amendment willingly and voluntarily; and they fully understand the terms, conditions, and obligations imposed by this Amendment.

21. Except as otherwise provided herein, all of the terms, covenants and conditions used herein shall have the meanings ascribed to them in the Manufacturing Agreement. In the event of a conflict among the terms and conditions of this Amendment and the Manufacturing Agreement, the following order of precedence shall prevail: (a) this Amendment; and (b) the Manufacturing Agreement.

AGREED AND APPROVED:

EMS

By: _____

Name: GREG JONES

Title DIRECTOR

HEWLETT-PACKARD COMPANY

By: ** _____

Name: **

Title: **

By: ** _____

Name: **

Title: **

RIC (Ramtron)

By: _____

Name: William Staunton

Title CEO

*Confidential treatment has been granted or requested with respect to portions of this exhibit, and such confidential portions have been deleted and separately filed with the Securities and Exchange Commission pursuant to Rule 24b-2 or Rule 406.

4.1.1 **Product Definition.** The HP Product will meet the specifications mutually agreed upon by EMS and HP. The agreed upon specifications are attached hereto as Exhibit R (the "Specifications"). Upon mutual agreement, the parties may amend add and/or modify the Specification, any such changes to be in writing and treated as an Amendment to the Manufacturing Agreement.

4.1.2 **Chip Design & Layout**. EMS will use all reasonable efforts to instruct HP personnel and/or HP's designees in the simulation methodologies and software tools used by EMS in the design of HP Products under the Pegasus Project. This training should cover the specifics of how such tools and methodologies have been used in the Pegasus Project; provided, however, that HP shall be responsible for obtaining instruction in the basic operation of tools identified by EMS where such training is available directly from the tool vendor. Training provided by EMS shall also include, but not be limited to, SPICE and/or other circuit simulations, Layout versus Schematic (LVS) verification tools, Design Rule Check (DRC) tools, and those tools used to generate any and all of the electronic files supplied to the Pegasus Project integrated circuit fabrication vendor.

EMS will deliver to HP electronic copies of all simulations (including, but not limited to, SPICE decks) used by EMS to verify correct operation of the design.

If further revisions to HP Products are required to meet the Specifications, the test time requirements (as set forth in Section 4.1.8 of Exhibit F-2)and/or the yield requirements (as set forth in Section 4.1.7 of Exhibit F-2) EMS shall assist HP in determining suitable modifications, verifying the correctness of such modifications via simulation and/or experimentation on existing material, and generating and transferring new design data to the HP-selected integrated circuit manufacturer. EMS shall also provide verification support to HP to enable HP and/or HP's designees to determine the effectiveness of any and all such modifications, EMS to use all reasonable efforts to provide verification support to HP as soon as any new Pegasus Project parts/revisions are available for evaluation.

4.1.3 **Test Program Development**. At all test points during the Pegasus Project, EMS shall participate with HP in creating electronic copies of all test plans and programs including, but not limited to: first wafer probe; post-fuse wafer probe; burn-in test vectors; and package test. All such tests must be designed and conducted to ensure that all Pegasus Project parts meet the Specifications, and the yield and test time goals (as such goals are set forth in Sections 4.1.7 and 4.1.8 of Exhibit F-2, below).

EMS will provide HP personnel and/or HP's designees with:

a. instruction and training regarding EMS' existing test plans and the methodologies used by EMS to deliver the required test flows to all subcontractors involved in the Pegasus Project; and

b. the details of the chip redundancy elements and how EMS uses test data and results to specify redundancy programming requirements to Pegasus Project integrated circuit fabrication vendor.

EMS and HP shall work together to complete the test development programs and plans as necessary to meet all Pegasus Project Specifications and the yield and test time goals (as such goals are set forth in Sections 4.1.7 and 4.1.8 of Exhibit F-2, below). In addition, EMS will work with HP to debug problems as described in Section 4.1.5 of Exhibit F-2, below, using wafer probe, package test, ebeam probe, FIB, and/or other techniques as required.

4.1.4 **Package Development**. EMS shall provide HP with any and all design specification, test and qualification data, and any and all special instructions related to package design and the support thereof, as such information is required by Project Pegasus packaging design and/or manufacturing subcontractor(s). In the event that a change to the package design is required to meet the Specifications contained in Exhibit R, EMS will participate with HP as necessary to both specify and qualify such

package design changes.

4.1.5 **Design Verification & Characterization Phase**. EMS shall work with HP to ensure that the Pegasus Project design and value chain is, and shall remain, robust across any and all integrated circuit manufacturing process variations which may occur over the manufacturing life of the HP Product. Robustness will be achieved in part by the evaluation of process window lots provided by the Pegasus Project integrated circuit manufacturer. In the event that any failure is discovered by either party which prevents or could prevent the HP Product from meeting the Pegasus Project Specifications or yield targets set forth in Exhibit R, then EMS shall use best efforts to provide those engineering resources necessary to modify the design and/or the value chain including, but not limited to, changes to test flow, programs and/or plans.

EMS shall work with HP to measure the sensitivity of the HP Product design to variations in internally generated supply voltages including, but not limited to, efforts to demonstrate the ability of the internally generated supply voltages to remain within the specified limits through any and all variations in process, temperature, external supply voltage, and access patterns.

EMS shall work with HP to debug failures as required to meet the Pegasus Project Specifications in Exhibit R, yield targets and/or reliability requirements. Such debugging may include, but is not limited to, addressing those failures (a) occurring during HP system testing, (b) occurring during margin testing, (c) detected at package test, (d) leading to excessive fallout at wafer probe, and (e) detected during reliability testing.

4.1.6 **Qualification**. EMS shall assist HP's evaluation of HP Product susceptibility to radiation-induced errors using models provided by the wafer foundry. Qualification testing includes HTOL, THB, ESD, Latch-Up, High Temperature Storage, Autoclave, Temperature cycling, Physical Dimensions, Moisture Stress, and Solderability. Burn-In Boards and THB Boards must be tooled to support all qualification testing. EMS may estimate soft error rate fail rates through accelerated testing and emission measurements from the lead-frame, mold compound and solder bumps.

4.1.7 **Product yield.** Pegasus Project parts shall achieve an Integrated Test Yield ("ITY") of at least sixty-five (65%) percent in accordance with the Specifications in Exhibit R. For the purposes of this Agreement, ITY shall mean the number of fully functional, full specification packaged parts expressed as a percentage of the total die produced by the integrated circuit fab. In addition, at least eighty-five (85%) percent of the Pegasus Project parts (measured on a monthly basis) which are packaged must pass all specified functional and electrical tests.

4.1.8 **Test time.** Production wafer test time shall not exceed thirty-five (35) seconds per part for a good die. Production final packaged part test time shall not exceed twenty (20) seconds per part for a good part.

4.1.9 **Additional Facilities.** EMS shall provide office space, network connections and telephones at the EMS facility in Colorado Springs for all HP personnel and/or HP's designees working on the Pegasus Project.

4.1.10 **Additional Offsite Support.** EMS shall work with HP as required to enable HP personnel and/or HP's designees to install and verify test flow releases performed at the facilities of the Pegasus Project's integrated circuit manufacturer and at the Pegasus Project's packaging contractor.

EXHIBIT N-2

Necessary Software and Hardware

- Design databases (schematics, artwork, package design documentation).
- Input decks and simulation files for Spice analysis.
- Substrate masks
- Burn-in board layout
- Spice Decks
- Tap estimations
- Package design
- Contact/revision information for s/w tools (Smartspice, Cadence).
- DUT board (the physical object and EMS information and documentation).
- Probe card (the physical object and vendor information and documentation).
- All test software - char/ver/test programs
- All production test software – wafer stress, fuse blow, pre & post fuse test, opens and shorts, hot & cold package test, wafer test and redundancy programming.
- Redundancy programming documentation.
- Existing/purchased prototype material (at EMS and in Infineon fab pipeline).
- Test chip (design files and existing/purchased material).
- Tester access information and documentation.
- All other Pegasus hardware, materials, documentation owned by EMS.
- Mebes database & physical masks
- All test data collected on Pegasus material at wafer and package test.

EXHIBIT P-2

EMS Key Personnel

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** (*)
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* as available to other project schedules

EXHIBIT Q-2

Equipment and Materials

1. EMS and RIC shall provide HP with access to equipment and materials located at the EMS facility in Colorado Springs (or at a RIC facility in Colorado) including, but not limited to, the following:

    21.1.1. Advantest 5592 Tester

    21.1.2. Probe Cards & Probecards

    21.1.3. Dut Boards

    21.1.4. Electroglas EG2001 Prober

    21.1.5. E-beam Prober (if available)

2. EMS and RIC shall immediately undertake whatever actions necessary to provide HP with access to the Advantest 5592 Tester equipment and materials located at an UTAC facility(ies).

3. EMS and RIC shall transfer to HP any and all rights held by EMS and/or RIC, now and in the future, to the following equipment and materials located at an UTAC facility(ies):

    21.1.6. Dut boards

    21.1.7. Burn-in Boards

    21.1.8. Bump Mask (FCD or Microfab)

    21.1.9. Sort Program

    21.1.10. Substrate & Mask database

    21.1.11. Backgrind program

    Prior to any transfer of the rights described in this Section 3, EMS and RIC shall make all payments owed and/or owing to UTAC so that such rights are transferred to HP free and clear of any and all encumbrances and/or payment obligations. EMS and RIC shall effectuate such transfer of rights to HP through novation, assignment or other means of transfer of EMS and/or RIC rights set forth in EMS' and/or RIC's agreements with UTAC.

4. EMS and RIC shall immediately undertake whatever actions necessary to arrange and facilitate HP's access to the Tester and Prober equipment and materials located at an Infineon facility(ies).

5. Subject to any pre-existing third party rights, EMS and RIC shall transfer to HP any and all rights held by EMS and/or RIC, now and in the future, to the following equipment and materials located at an Infineon facility(ies):

    21.1.12. Wafer masks & database

    21.1.13. Probe Cards

EXHIBIT R

Project Pegasus Specifications

Exhibit R – Part 1 - 72Mbit DDR ESRAM 2Mx36

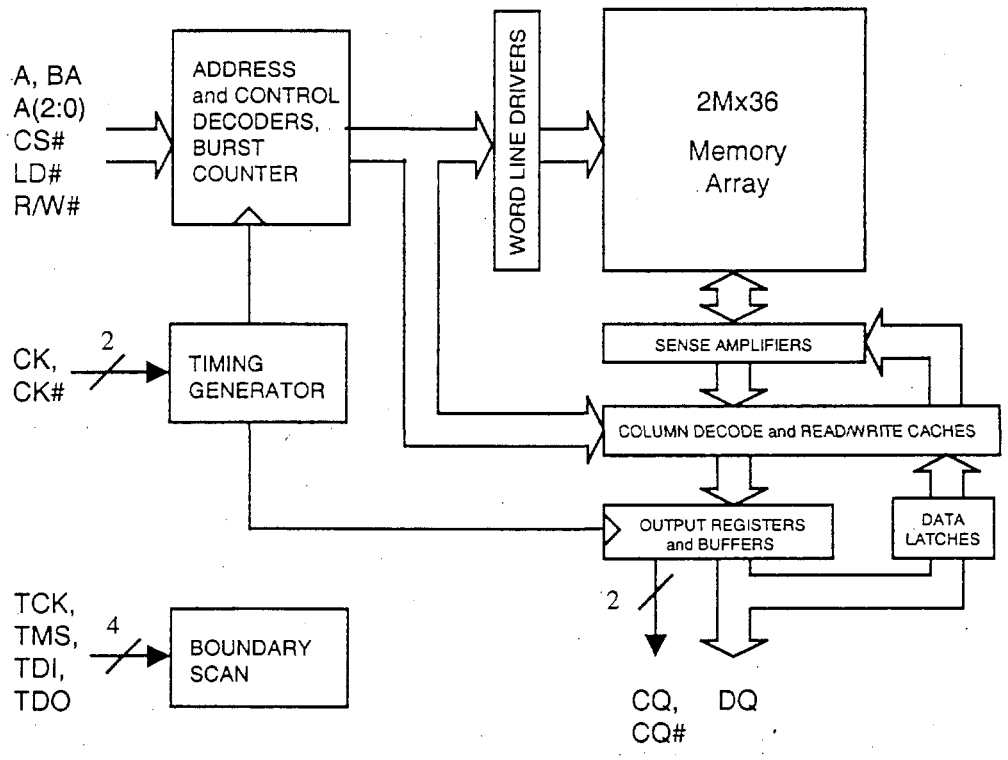
Features

- 72Mbit Density
- 333 MHz Clock Rate, 666 Mbps Data Rate
- Low Latency Cached DRAM Architecture
- Pin Selectable Read/Write Latency
- Burst Length of Eight
- Coherent Late Writes
- Single 2.5V Power Supply
- Low Power 1.2V HSTL I/O Interface
- Differential Echo Clock Outputs
- Programmable Output Impedance Drivers
- JEDEC Standard 209-ball PBGA Package
  - 14 x 22 mm Body Size
  - 1.0 mm Ball Pitch, 11 x 19 Array
  - 1.65 mm (max) Package Height
  - Flip-Chip Die Attach

Description

The Enhanced Memory Systems SS2615 DDR ESRAM is a 72Mbit double data rate I/O memory device that combines raw speed with innovative architecture to optimize system price/performance in high performance cache memory and communications systems. The device is packaged in a JEDEC standard 209-ball plastic BGA. The SS2615 achieves a bandwidth of 3.0 GB/s while maintaining a low initial access of 13 ns. An equivalent serial data rate is 24 Gb/s. The memory arrays are organized in sixteen independent banks, which allow a pseudo-random address cycle time of 13 ns.

FUNCTIONAL BLOCK DIAGRAM



- Multilayer Substrate includes Ground Plane

Pin Assignments (Top View)

SS2615
2Mx36
209-ball PBGA

	1	2	3	4	5	6	7	8	9	10	11
A	VSS	VDDQ	VSS	A	VSS	VREF	VSS	A	VSS	VDDQ	VSS
B	DQ	DQ	DQ	VSS	A	VSS	A	VSS	NC	NC	NC
C	NC	NC	NC	VSS	A	LD#	A	VSS	DQ	DQ	DQ
D	VSS	VDDQ	VSS	VDD	A	VSS	A	VDD	VSS	VDDQ	VSS
E	DQ	DQ	DQ	VSS	BA	R/W#	BA	VSS	NC	NC	NC
F	NC	NC	NC	VDD	BA	CS#	BA	VDD	DQ	DQ	DQ
G	VSS	VDDQ	VSS	VDD	VSS	VSS	VSS	VDD	VSS	VDDQ	VSS
H	DQ	DQ	DQ	VSS	CK	NC	NC	VSS	NC	NC	NC
J	NC	NC	NC	VSS	CK#	M1	NC	VSS	DQ	DQ	DQ
K	VSS	VDDQ	VSS	VDD	VSS	VSS	VSS	VDD	VSS	VDDQ	VSS
L	DQ	DQ	DQ	VSS	CQ	VSS	NC	VSS	NC	NC	NC
M	NC	NC	NC	VSS	CQ#	VSS	NC	VSS	DQ	DQ	DQ
N	VSS	VDDQ	VSS	VDD	VSS	VSS	VSS	VDD	VSS	VDDQ	VSS
P	DQ	DQ	DQ	VDD	ZQ	NC	NC	VDD	NC	NC	NC
R	NC	NC	NC	VSS	A	NC, A	A	VSS	DQ	DQ	DQ
T	VSS	VDDQ	VSS	VDD	VSS	VSS	VSS	VDD	VSS	VDDQ	VSS
U	DQ	DQ	DQ	VSS	A	A2	A	VSS	NC	NC	NC
V	NC	NC	NC	TMS	A	A1	A	TCK	DQ	DQ	DQ
W	VSS	VDDQ	VSS	TDI	VSS	A0	VSS	TDO	VSS	VDDQ	VSS

NOTE: Location 6R is the expansion address for a future 144Mb device.

Pin Descriptions

Symbol	Type	Function
CK, CK#	Input	Input Clock: All input signals are sampled on the rising edge of CK and the falling edge of CK#, where CK and CK# voltage levels cross.
CS#	Input	Chip Select: This active low synchronous input is registered when LD# is low, otherwise ignored. When LD# is registered low and chip select is registered low, the chip begins a read or write cycle. When LD# is registered low and chip select is registered high, the chip begins a deselect cycle.
LD#	Input	Load Address: Active low LD# latches the address, and decodes the R/W#. When LD# is registered high, the device internally increments the A(2:0) address that was initially latched.
R/W#	Input	Read/Write Input: This signal determines whether to start a read or write cycle only when both CS# and LD# are registered low.
A(2:0)	Input	Burst Address Inputs: These inputs are registered when CS# and LD# are low, otherwise they are ignored. They define the starting address within a cache line boundary. The burst wrap sequence is defined in the Burst Wrap Sequence Table.
A, BA	Input	Address Inputs: These address inputs are registered when CS# and LD# are low, otherwise they are ignored. The BA bank address pins determine which one of the sixteen internal banks is accessed.
DQ	Input/ Output	Data I/O: Data bus inputs and outputs. For read cycles, the device drives output data on these pins after the read latency is satisfied. Read data is edge aligned with the output clocks CQ and CQ#. At the completion of the burst read cycle, the device automatically places the output buffers in hi-Z. For write cycles, input data is applied to these pins and must be set-up and held relative to the rising and falling edge of clock CK.
CQ, CQ#	Output	Output Clock: These free running output clocks are used to capture read data at the memory *controller using CQ and CQ# as a timing reference. Read data driven on the DQ pins is valid on the* rising and falling edges of CQ and CQ#, where CQ and CQ# voltage levels cross.
ZQ	Input	Output Impedance Control: An RQ resistor must be connected between ZQ and V_{SS}. The resistor value defines the DQ output driver impedance. RQ must be chosen such that it is 5 times the desired driver impedance.
M1	Input	Mode 1 Input: This static input defines read/write latency. If high, the read/write latency is 6 clocks. If low, the read/write latency is 4 clocks.
TCK	Input	Test Clock: Input clock for boundary scan. If boundary scan is not used, TCK must be tied to either V_{DD} or V_{SS}.
TMS	Input	Test Mode Select: This input controls the TAP controller and is sampled on the rising edge of TCK.
TDI	Input	Test Data In: This is the serial data input for boundary scan testing.
TDO	Output	Test Data Out: This is the serial data output for boundary scan testing.
V_{REF}	Supply	Reference power supply for input buffers.
V_{DD}, V_{SS}	Supply	Power (+2.5V) and ground for the input buffers and core logic.
V_{DDQ}	Supply	Isolated power supply for I/O interface (DQ). V_{DDQ} must be connected to 1.2V power.
NC	-	No Connect: These pins do not connect to the chip.

Device Operation

The Enhanced Memory Systems SS2615 ESRAM is a DRAM-based DDR SRAM equivalent. The device is a burstable read/write memory with a double data rate (DDR) interface. Read and write transactions always have a burst length of eight. Burst cycles cannot be interrupted. Once the burst length is satisfied, the device automatically hi-Z's the data bus on reads and ignores the data bus on writes. The M1 pin selects the initial read and write data latency as either 4 clocks or 6 clocks.

The device is internally organized as sixteen banks. This allows most accesses to be serviced on as few as four clock boundaries since the only timing constraint imposed on alternate bank accesses is one that ensures read and write bursts are not interrupted.

Burst Read Accesses

A read cycle is initiated on the rising edge of clock CK when CS# and LD# are registered low and R/W# is registered high. The first beat of read data is driven on the data bus 4 (M1 low) or 6 (M1 high) clocks following the read address. Output data is valid coincident with the output clocks CQ and CQ#. For improved data bus signal integrity, the eighth beat of read data is extended an extra data phase. The exception to this rule occurs when an alternate bank read access allows back-to-back read bursts without interruption. See Timing Diagrams section for details.

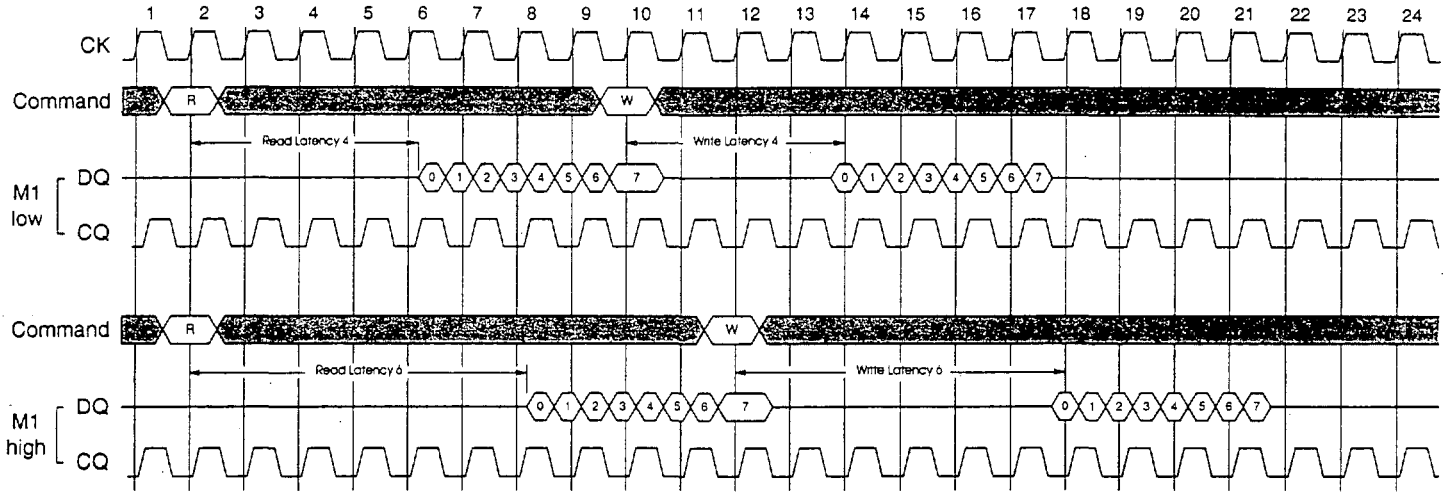
Burst Write Accesses

A write cycle is initiated when CS#, LD#, and R/W# are all registered low on the rising edge of clock CK. Write data latency is 4 or 6 clocks dependent on the M1 setting. Input data is referenced to the device's input clocks CK and CK#.

Burst Wrap Sequence

Start Address			Interleaved
A2	A1	A0	(decimal)
0	0	0	0, 1, 2, 3, 4, 5, 6, 7
0	0	1	1, 0, 3, 2, 5, 4, 7, 6
0	1	0	2, 3, 0, 1, 6, 7, 4, 5
0	1	1	3, 2, 1, 0, 7, 6, 5, 4
1	0	0	4, 5, 6, 7, 0, 1, 2, 3
1	0	1	5, 4, 7, 6, 1, 0, 3, 2
1	1	0	6, 7, 4, 5, 2, 3, 0, 1
1	1	1	7, 6, 5, 4, 3, 2, 1, 0

Pin Programmable Latency (M1 Pin)



Device Deselect (Refresh)

A deselect cycle is initiated when CS# is registered high and LD# is registered low. All address inputs are ignored. Once the Deselect command is issued, the device is unavailable for a read or write cycle until the minimum bank cycle time is satisfied (t_{RC}). A requirement of 4,096 deselect cycles every 16 ms is necessary to maintain data integrity in the memory arrays. This corresponds to Deselect commands being evenly distributed every 3.9 µs. Since some system designs require flexibility in timing Deselect commands, the device allows a reduced time interval of 1.5 µs between Deselect commands. Output buffer (DQ) impedance updates occur during deselect cycles.

No Operation

Once a burst cycle completes and LD# is registered high on the rising edge of clock CK, the device performs a no operation cycle.

Truth Table

Operation	CS#	LD#	R/W#	Address	Action
Burst Read	L	L	H	Start Address	Start bursting data out on 4th or 6th clock.
Burst Write	L	L	L	Start Address	Start bursting data in on 4th or 6th clock.
Device Deselect	H	L	X	X	Refresh cycle begins and completes in 8 or 10 clocks.
No Operation	X	H	X	X	If burst is complete, device remains idle.

Electrical Characteristics

Absolute Maximum Ratings

Description	Symbol	Value
Power Supply Voltage	V_{DD}	-0.5V to +3.5V
I/O Power Supply Voltage	V_{DDQ}	-0.5V to +2.5V, where $V_{DDQ} \leq V_{DD}$+0.5V
Voltage on any Pin with Respect to Ground	V_{IN}, V_{OUT}	-0.5V to +2.65V
Junction Temperature	T_J	110°C
Storage Temperature	T_{STG}	-55°C to +125°C
DC Output Current (I/O pins)	I_{OUT}	±50mA

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these, or any other conditions above those listed in the operational section of the specification, is not implied. Exposure to conditions at absolute maximum ratings for extended periods may affect device reliability.

DC Characteristics (T_C = 0°C to +90°C)

Symbol	Parameter	Min	Typical	Max	Units	Notes
V_{DD}	Supply Voltage	2.4	2.5	2.65	V	
V_{DDQ}	I/O Supply Voltage	1.1	1.2	1.3	V	
V_{IH}	Input High Voltage (excluding CK,CK#)	V_{REF}+0.1	-	1.6	V	
V_{IL}	Input Low Voltage (excluding CK, CK#)	-0.3	-	V_{REF}-0.1	V	1
V_{CK}	Clock Input Voltage	-0.3	-	1.6	V	
V_{CKH}	Clock Input High Level	V_{REF}+0.2	-	1.6	V	4
V_{DF}	Clock Input Differential Voltage	0.4	-	1.9	V	3
V_{CM}	Clock Input Common Mode Voltage Range	0.4	-	0.8	V	1
V_{REF}	Input Reference Voltage	0.4	-	0.8	V	
I_{ILK}	Input Leakage Current	-	-	±2	µA	
I_{OLK}	Output Leakage Current	-	-	±5	µA	
I_{OH}	Output High Current ($V_O = V_{DDQ}/2$, $R_Q = 200\ \Omega$)	12.5	-	18.0	mA	2
I_{OL}	Output Low Current ($V_O = V_{DDQ}/2$, $R_Q = 200\ \Omega$)	12.5	-	18.0	mA	2

Notes:

1. V_{IL} minimum is –0.7V for ≤ 1ns.
2. I_{OH} and I_{OL} test limits are intended to guarantee the DC value of the driver output impedance of 40 ohms ± 10%. Minimum limit is defined by $[(V_{DDQ} / 2) / (R_Q / 5 + 10\%)]$. Maximum limit is defined by $[(V_{DDQ} / 2) / (R_Q / 5 - 10\%)]$.
3. V_{DF} max. is equal to V_{CK} max. of one clock signal minus V_{CK} min. of the other clock signal.
4. Clock high pulse width measured at V_{CKH} must be at least 1.0 ns.

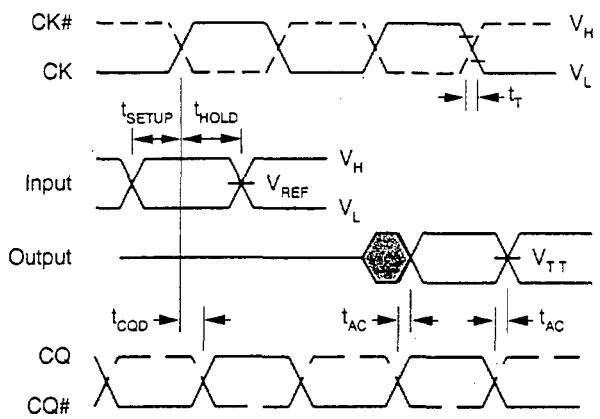
Power Supply Currents (T_C = 0°C to +90°C, 2.4V ≤ V_{DD} ≤ 2.65V)

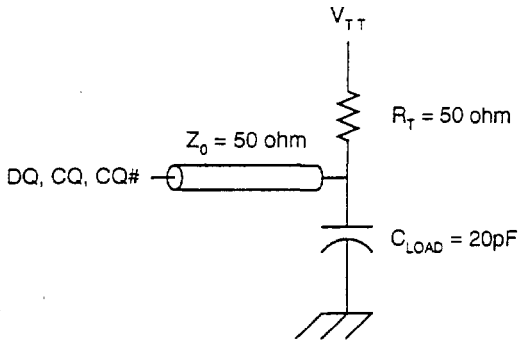
Symbol	Parameter	-3.0		-3.6		-4.5		Units	Notes
		Min	Max	Min	Max	Min	Max		
I_{DD}	Average Operating Current (Read/Write command every 4 clocks, accessing alternate internal banks)	-	680	-	650	-	550	mA	
I_{SB}	Standby Current (No Read/Write commands, Deselect command issued every 3.9 µs)	-	430	-	400	-	375	mA	

Package Thermal Characteristics

Symbol	Parameter	Value	Units	Notes
θ_{JB}	Thermal Resistance (Junction to Solder Balls)	14	°C/W	
θ_{JC}	Thermal Resistance (Junction to Case)	5	°C/W	

AC Test Conditions (T_C = 0°C to +90°C)





AC Output Load Curcuit

1. An initial pause of 500µs is required after power-up.
2. AC test output timings are referenced to $V_{TT} = (V_{DDQ} / 2)$.
3. AC inputs use V_L = 0V, $V_H = V_{DDQ}$, V_{REF} = 0.6V, and input timings are referenced to V_{REF}.
4. The transition time is measured between 20% and 80%.
5. AC test measurements assume t_T = 0.5ns.
6. In addition to meeting the transition rate specification, the clock must transit between V_H and V_L (or between V_L and V_H) in a monotonic manner.
7. Access time for the first data word following a hi-Z condition is guaranteed not only from a $V_{TT} = (V_{DDQ} / 2)$ condition, but also from a V_{DDQ} and V_{SS} condition as well.

Capacitance (T_C = 25°C, f = 100MHz, 2.4V ≤ V_{DD} ≤ 2.65V, V_{DDQ} = 1.2V ± 0.1V)

Symbol	Parameter	Min	Typical	Max	Units	Notes
C_{CK}	Input Clock Capacitance (CK, CK#)	5.0	-	8.5	pF	1
C_{IN}	Input Capacitance (Address, Control)	3.0	4.0	5.0	pF	1
C_O	Output Capacitance (DQ)	4.0	5.0	6.0	pF	1
C_{VR}	V_{REF} Input Capacitance	100	-	-	pF	1

Notes:
1. Value includes package capacitance.

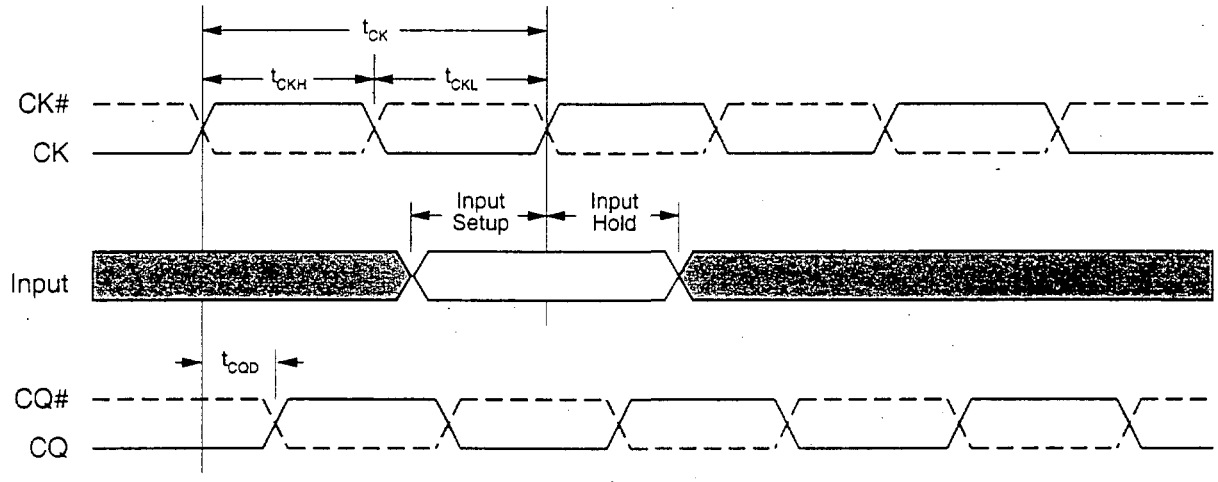
AC Operating Conditions (T_C = 0°C to +90°C)

Clock

Symbol	Parameter	-3.0		-3.6		-4.5		Units	Notes
		Min	Max	Min	Max	Min	Max		
f_{CK}	Clock Frequency	100	333	100	278	100	220	MHz	
t_{CK}	Clock Cycle Time	3.0	10	3.6	10	4.5	10	ns	
t_{CKH}	Clock High Time	1.5	-	1.7	-	2.0	-	ns	1, 2
t_{CKL}	Clock Low Time	1.5	-	1.7	-	2.0	-	ns	1, 2
t_{CKDC}	Clock Duty Cycle	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	3
t_{CQD}	CK Clock to CQ Clock Delay Time	1.6	2.5	1.6	2.5	1.6	3.0	ns	1, 2

Notes:
1. Access time is measured at $V_{TT} = (V_{DDQ} / 2)$. See AC Test Load.
2. Assumes clock rise and fall times are equal to 0.5ns.
3. This parameter is specified to ensure reasonable duty cycles at frequencies below f_{CK} (max).

Clock and Input Timing



Common Parameters

Symbol	Parameter	-3.0		-3.6		-4.5		Units	Notes
		Min	Max	Min	Max	Min	Max		
t_{CS}	Command and Address Set-Up Time	1.0	-	1.0	-	1.4	-	ns	
t_{CH}	Command and Address Hold Time	0.33	-	0.33	-	0.5	-	ns	4
t_{AH}	Burst Address (A0-A2) Hold Time	0.5	-	0.5	-	0.8	-	ns	
t_{RC1}	Read/Write Bank Cycle Time (M1 low)	24.0	-	28.8	-	36.0	-	ns	1
t_{RC2}	Read/Write Bank Cycle Time (M1 high)	30.0	-	36.0	-	45.0	-	ns	2
t_{REF}	Deselect Time Interval	1.5	-	1.5	-	1.5	-	µs	3

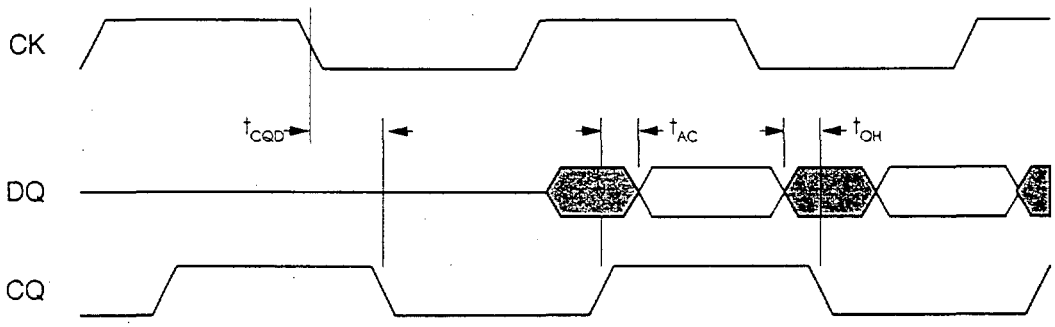
Notes:
1. When M1 is low, read/write latencies are four clocks.
2. When M1 is high, read/write latencies are six clocks.
3. The memory controller must issue at least 4,096 deselect commands every 16 ms.
4. Except A0-A2 address inputs.

Read and Write Parameters

Symbol	Parameter	-3.0		-3.6		-4.5		Units	Notes
		Min	Max	Min	Max	Min	Max		
t_{AC}	Clock Access Time (ref to CQ)	-	0.33	-	0.33	-	0.5	ns	1, 2
t_{OH}	Output Hold Time (ref to CQ)	-0.33	-	-0.33	-	-0.5	-	ns	1, 2
t_R, t_F	Output Rise/Fall Time	-	0.8	-	0.8	-	1.2	ns	3, 4
t_{DS}	Data Input Set-Up Time	0.33	-	0.33	-	0.5	-	ns	4
t_{DH}	Data Input Hold Time	0.33	-	0.33	-	0.5	-	ns	4

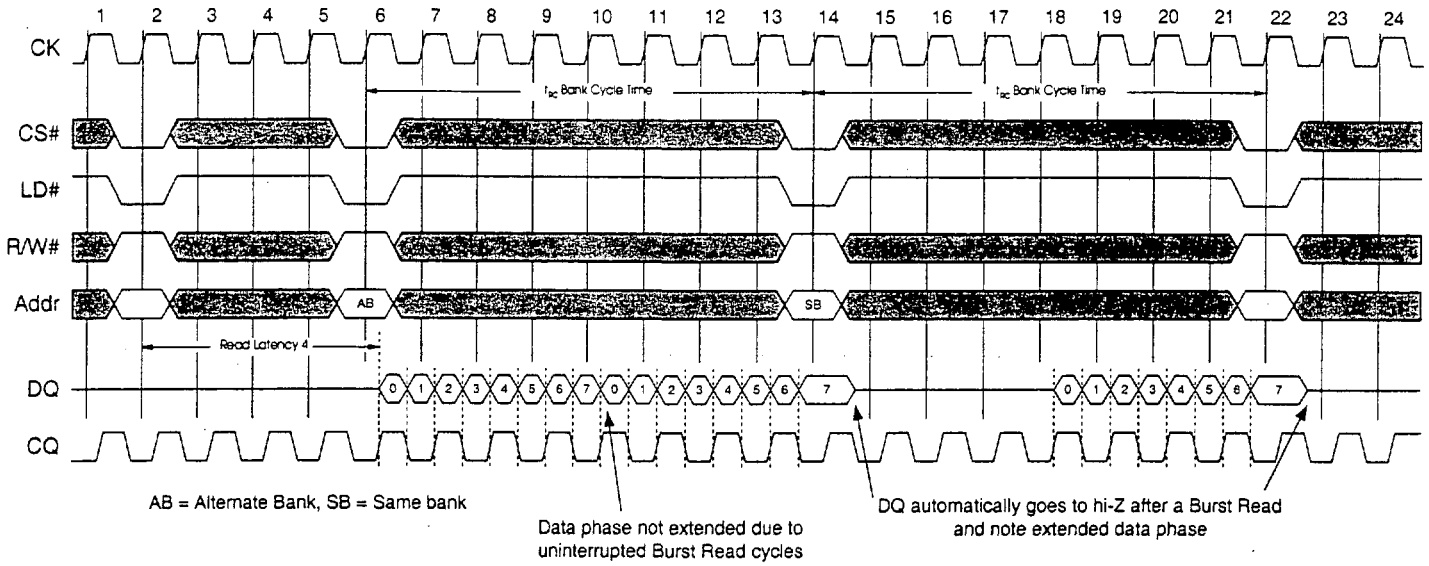
Notes:
1. Access time is measured at $V_{TT} = (V_{DDQ} / 2)$. See AC Test Load.
2. Assumes clock rise and fall times are equal to 0.5ns.
3. Based on a 10% to 90% measurement.
4. Guaranteed by design and characterization.

Read Parameter Timing

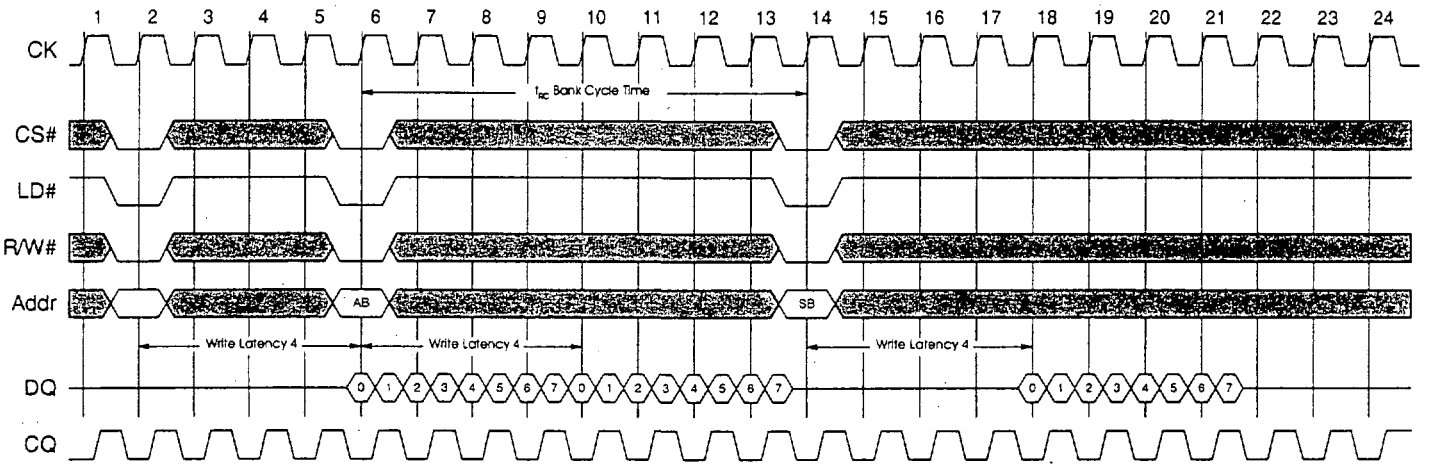


Timing Diagrams

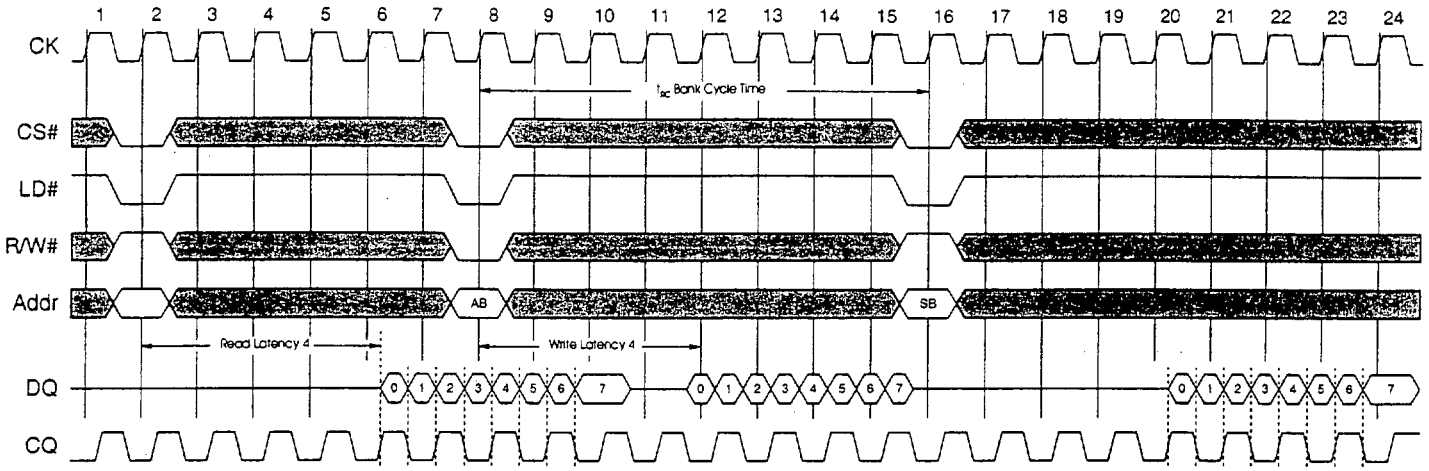
Burst Reads (Latency 4)



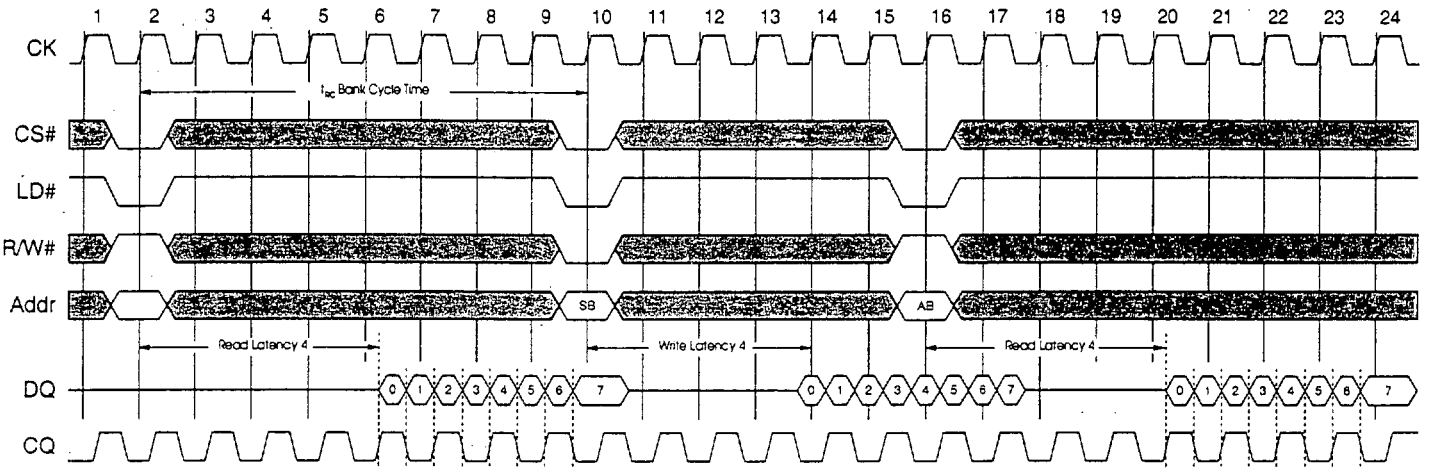
Burst Writes (Latency 4)



Burst Read/Write/Read (Latency 4)

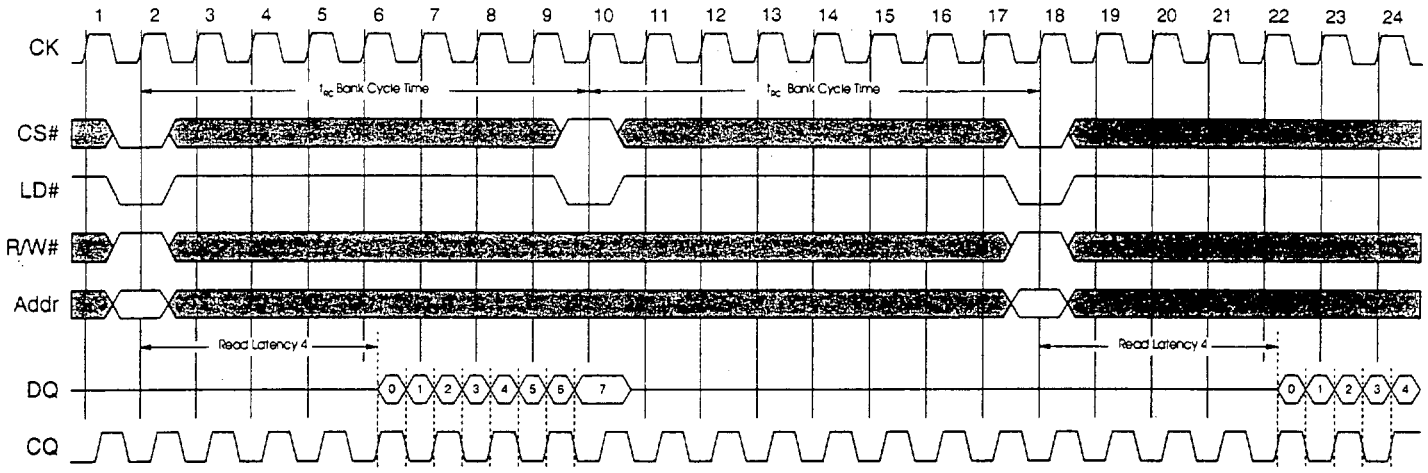


AB = Alternate Bank, SB = Same bank

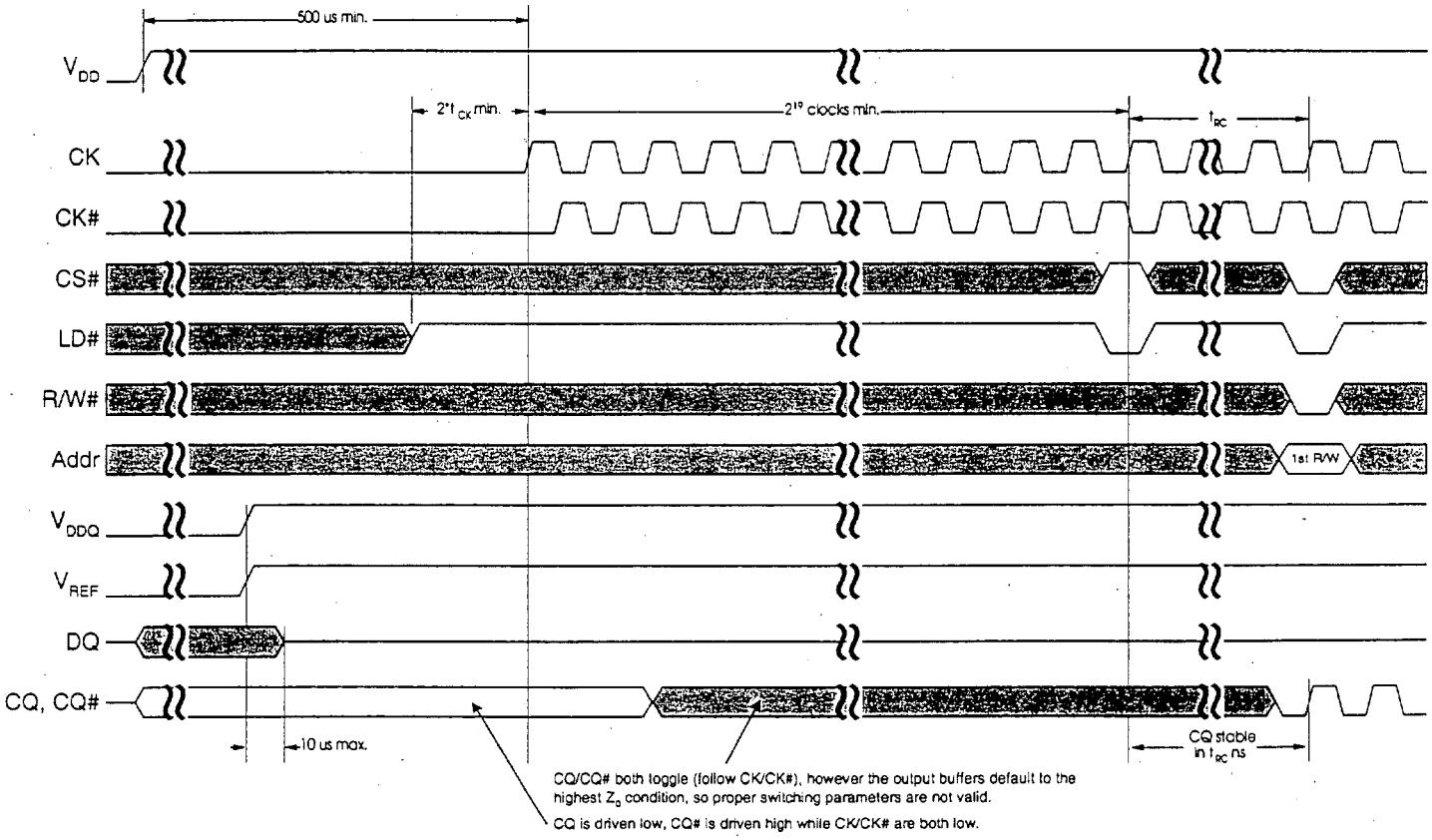


AB = Alternate Bank, SB = Same bank

Deselect (Refresh) Cycle between Random Reads



Power-Up and Initialization



IEEE 1149.1 Serial Boundary Scan (JTAG)

The SS2615 includes a serial boundary scan Test Access Port (TAP). This port functions in accordance with IEEE Standard 1149.1-1990, but does not have the set of functions required for full 1149.1 compliance. These functions are excluded because they place an added delay in the critical speed path of the device's inputs and outputs. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices that use 1149.1 fully compliant TAPs.

Disabling the JTAG Feature

The SS2615 can operate normally without using the JTAG feature. At power-up, the TAP controller is placed in a reset state and does not interfere with device operation. To ensure the TAP controller is disabled, tie TCK to either V_{SS} or V_{DD}. This prevents the TAP controller from operating even if TMS toggles.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. This pin is pulled up internally.

Test Data In (TDI)

The TDI pin is used to serially input information to the registers. It can be connected to the input of any of the registers. Which register is placed between TDI and TDO is determined by the instruction loaded into the TAP Instruction register. See the TAP Controller State Diagram for more information. TDI is internally pulled up and can be unconnected if the TAP is unused. TDI is connected to the most significant bit (MSB) on any register.

Test Data-Out (TDO)

The TDO output is used to serially output information from the registers. The output is active depending on the current state of the TAP state machine. See the TAP Controller State Diagram for more information. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any selected register. If the JTAG feature is not used, TDO should be left unconnected.

Performing a TAP Reset

A TAP reset is performed by forcing TMS high for five rising edges of TCK. This reset does not affect the operation of the device and may be performed while the device is operating. At power-up, the TAP is reset internally to ensure that TDO comes up in a high-Z state.

TAP Registers

Registers are connected between the TDI and TDO pins and allow scanning of data into and out of the SS2615 test circuitry. Only one register can be selected at a time through the Instruction register. Data is serially loaded through the TDI pin on the rising edge of TCK and is driven out through the TDO pin on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the Instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in the TAP Controller Block Diagram. At power-up, the Instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section "Performing a TAP Reset".

When the TAP controller is placed in the Capture-IR state, the two least significant bits are loaded with a binary "01" pattern to allow for fault isolation of the board level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The Bypass register is a single-bit register that can be placed between the TDI and TDO pin, allowing data to shift through the device with minimal delay. The Bypass register is set low when the Bypass instruction is executed.

Boundary Scan Register

This register is connected to all input and output pins on the SS2615.

The Boundary Scan register is loaded with the current states on the inputs and outputs of the pad ring when the TAP controller enters the Capture-DR state. The register is then serially placed between the TDI and TDO pins when the controller enters the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE-Z instructions can be used to capture the contents of the pad ring.

The Boundary Scan Order table shows the order in which the bits are connected. Each bit corresponds to one of the solder balls on the package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the Instruction register. The IDCODE is hardwired into the device and can be shifted out when the TAP controller is placed in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP Instruction Set

Eight different instructions are possible with the 3-bit Instruction register. All combinations are listed in the Instruction Code table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described below.

The TAP controller used in this device is not fully compliant with the 1149.1 conventions because some of the mandatory instructions are not fully implemented. The TAP controller cannot be used to load address, data, or control signals into the ESRAM, and cannot preload the Input or Output buffers. This device does not implement the following instructions as specified by the 1149.1 standard: EXTEST, INTEST, or the PRELOAD portion of SAMPLE/PRELOAD. Instead it captures the current states on the inputs and outputs of the pad ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the Instruction register is placed between TDI and TDO. During this state, instructions are shifted through the Instruction register through the TDI and TDO pins. To execute the instruction once it is shifted in, the TAP controller is moved into the Update-IR state.

EXTEST

When the EXTEST instruction is loaded into the Instruction register, the SS2615 places all outputs (DQ, CQ, and CQ#) into a high-Z state. The EXTEST instruction is executed when the Instruction register is loaded with all 0's. The EXTEST instruction places the Boundary Scan register between the TDI and TDO pins when the TAP controller enters a Shift-DR state. When the TAP controller is placed in the Capture-DR state, a snapshot of data on the input and output pins is captured in the Boundary Scan register. The CK, CK#, CQ, and CQ# pins are each captured single-ended.

EXTEST is a mandatory 1149.1 instruction. EXTEST is not implemented in the TAP controller as specified in the 1149.1 standard. Therefore, this device is not fully compliant with the 1149.1 standard.

IDCODE

The IDCODE instruction causes a vendor specific, 32-bit code to load into the ID register. It also places the ID register between the TDI and TDO pins, and allows shifting of the IDCODE out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the Instruction register at power up or when the TAP controller is given a TEST-LOGIC RESET state.

SAMPLE-Z

The SAMPLE-Z instruction places the Boundary Scan register between the TDI and TDO pins when the TAP controller enters a Shift-DR state. It also places all outputs (DQ, CQ, and CQ#) into a high-Z state.

SAMPLE/PRELOAD

When the SAMPLE/PRELOAD instruction is loaded into the Instruction register and the TAP controller is placed in the Capture-DR state, a snapshot of data on the input and output pins is captured in the Boundary Scan register.

Note that the TAP controller clock TCK operates at a frequency up to 10 MHz, while the main clocks CK/CK# operate at more than an order of magnitude faster. Because of this, it is possible for an input or output to change during the Capture-DR state. If the TAP tries to capture a signal while it is transitioning (metastable state), the device is not harmed, but the results are not guaranteed and possibly not repeatable.

To guarantee that the Boundary Scan register captures the correct value, the signal must be stable long enough to meet TAP controller capture set-up and hold times (t_{CS} and t_{CH}). To capture the clock inputs

correctly, there must be a way to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is not done in the design, it is still possible to capture all other signals and simply ignore the value of CK/CK# captured in the Boundary Scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the Boundary Scan register between the TDI and TDO pins.

SAMPLE/PRELOAD is a mandatory 1149.1 instruction. The PRELOAD portion of this instruction is not implemented, so the TAP controller is not fully compliant with the 1149.1 standard.

Note that since the PRELOAD part of this instruction is not implemented, placing the TAP into the Update-DR state while performing a SAMPLE/PRELOAD instruction has the same effect as the Pause-DR instruction.

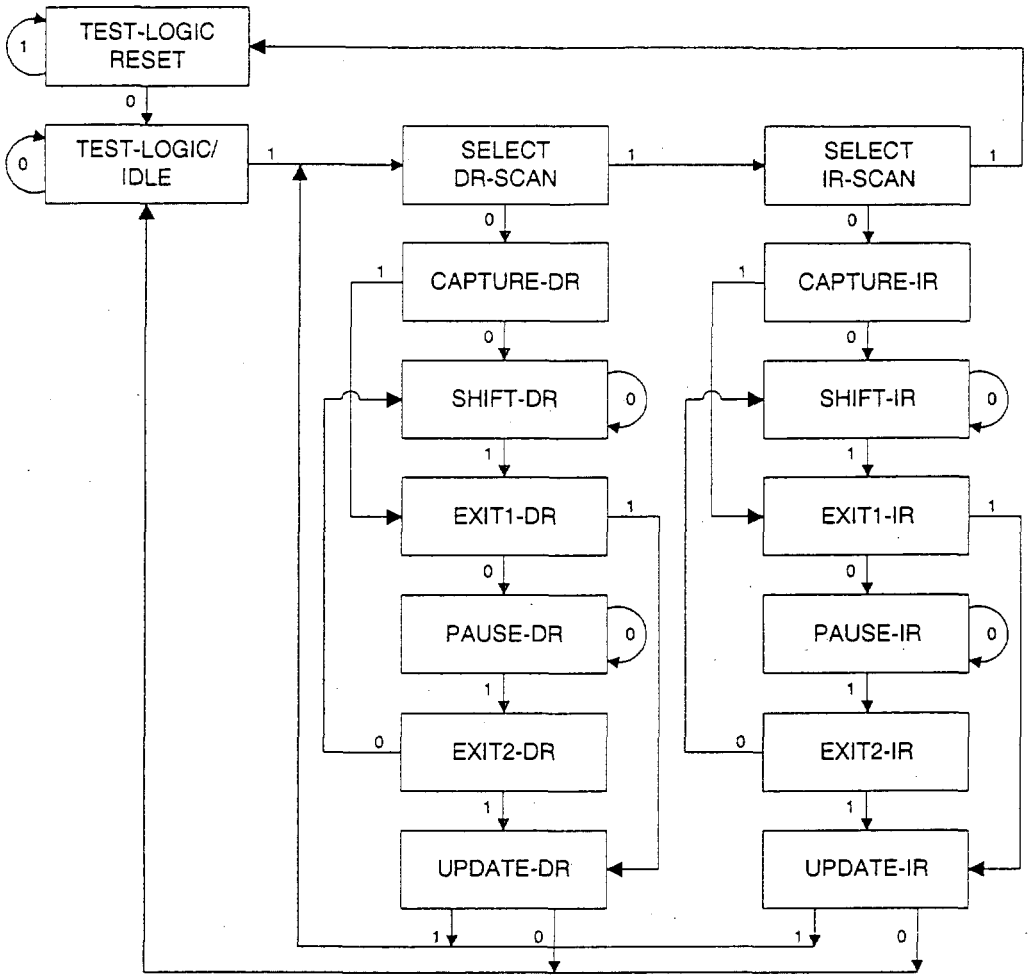
BYPASS

When the BYPASS instruction is loaded in the Instruction register and the TAP is placed in a Shift-DR state, the Bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

RESERVED

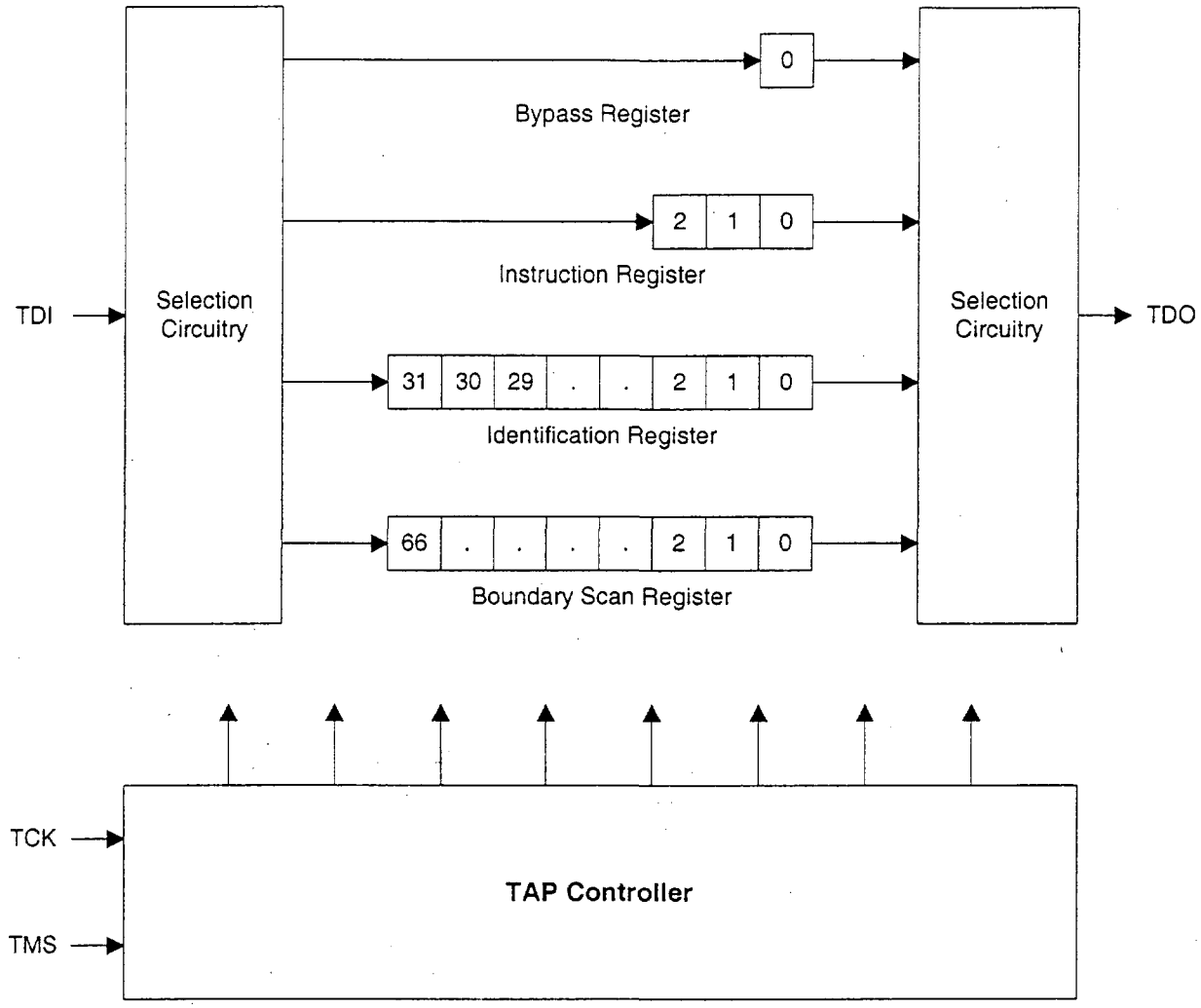
These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Controller State Diagram



NOTE: The 0 or 1 next to each state represents the TMS signal value at the rising edge of TCK.

TAP Controller Block Diagram



TAP DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Min	Max	Units	Notes
V_{OH}	Output High Voltage	I_{OH} = -2.0 mA	2.0	-	V	1
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA	-	0.4	V	1
V_{IH}	Input High Voltage	–	1.7	V_{DD}+0.3	V	1, 2
V_{IL}	Input Low Voltage	–	-0.3	0.7	V	1, 2
I_X	Input and Output Leakage Current	GND ≤ V_{IN} ≤ V_{DD}	-	±5	µA	1, 3

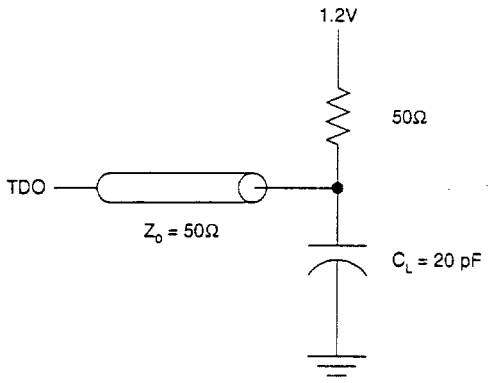
Notes:
1. All voltage referenced to ground.
2. Overshoot: $V_{IH}(AC) \leq V_{DD}+0.5V$ for $t \leq (t_{TCYC} / 2)$,
   Undershoot: $V_{IL}(AC) \leq 0.5V$ for $t \leq (t_{TCYC} / 2)$.
3. Value accounts for input ` ull-ups on TMS and TDI pins.

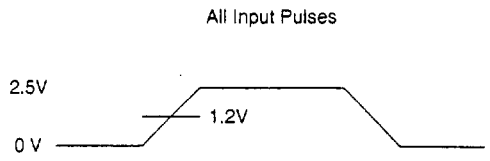
TAP AC Switching Characteristics

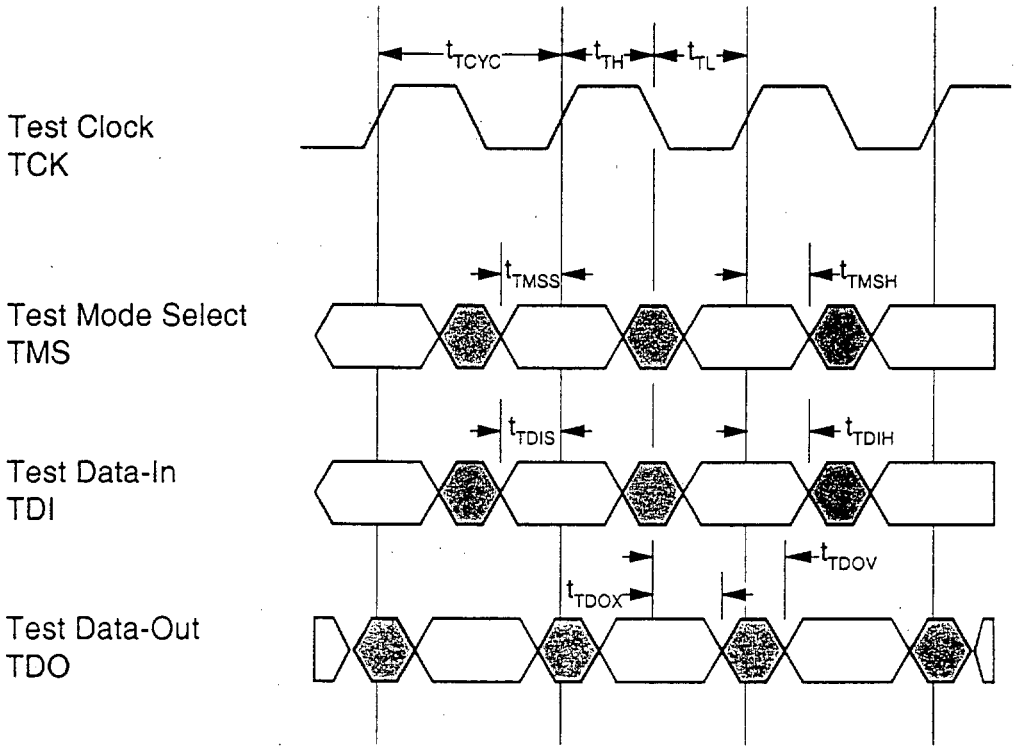
Symbol	Parameter	Min	Max	Units	Notes
t_{TCYC}	TCK Clock Cycle Time	100	-	ns	1
t_{TF}	TCK Clock Frequency	-	10	MHz	1
t_{TH}	TCK Clock High	40	-	ns	1
t_{TL}	TCK Clock Low	40	-	ns	1
t_{TMSS}	TMS Setup to TCK Clock Rise	10	-	ns	1
t_{TDIS}	TDI Setup to TCK Clock Rise	10	-	ns	1
t_{CS}	Capture Setup to TCK Clock Rise	10	-	ns	1, 2
t_{TMSH}	TMS Hold after TCK Clock Rise	10	-	ns	1
t_{TDIH}	TDI Hold after Clock Rise	10	-	ns	1
t_{CH}	Capture Hold after Clock Rise	10	-	ns	1, 2
t_{TDOV}	TCK Clock Low to TDO Valid	-	20	ns	1
t_{TDOX}	TCK Clock Low to TDO Invalid	0	-	ns	1

Notes:
1. Test conditions are specified using the loads in TAP AC test conditions. T_R/t_F = 1 ns.
2. t_{CS} and t_{CH} refer to the setup and hold time requirements for latching data from the Boundary Scan register.

TAP Timing and Test Conditions







Boundary Scan Order

Scan Bit #	Signal Name	BGA Pin Location	Scan Bit #	Signal Name	BGA Pin Location	Scan Bit #	Signal Name	BGA Pin Location
0	DQ	9V	25	A	7C	50	LD#	6C
1	DQ	10V	26	A	8A	51	CS#	6F
2	DQ	11V	27	DQ	9J	52	CK	5H
3	DQ	10R	28	DQ	10J	53	CK#	5J
4	DQ	11R	29	DQ	11J	54	CQ	5L
5	DQ	9R	30	DQ	10F	55	CQ#	5M
6	DQ	10M	31	DQ	9F	56	A	5U
7	DQ	11M	32	DQ	11F	57	A	5V
8	DQ	9M	33	DQ	10C	58	DQ	3L
9	A	7V	34	DQ	11C	59	DQ	1L
10	A	7U	35	DQ	9C	60	DQ	2L
11	A2	6U	36	DQ	3B	61	DQ	2P
12	A	7R	37	DQ	2B	62	DQ	3P
13	A1	6V	38	DQ	1B	63	DQ	1P
14	A	5R	39	DQ	2E	64	DQ	2U
15	A0	6W	40	DQ	3E	65	DQ	1U
16	M1	6J	41	DQ	1E	66	DQ	3U
17	CK#	5J	42	DQ	2H			
18	CK	5H	43	DQ	1H			
19	BA	5E	44	DQ	3H			
20	R/W#	6E	45	A	4A			
21	BA	7F	46	A	7B			
22	A	5D	47	A	5C			
23	A	7D	48	BA	5F			
24	BA	7E	49	A	5B			

Identification Register Definitions

Instruction Field	Value	Description
Revision Number (31:29)	XXX	Defines die revision number.
Voltage (28,24)	0, 1	Defines V_{DD} voltage (2.5V).
Reserved (27:25)	XXX	Reserved.
Architecture (23:21)	110	Defines DDR **E**SRAM architecture
Memory Type (20:18)	100	Defines type of **E**SRAM (burst 8)
Bus Width (17:15)	100	Defines width (x36)
Density (14:12)	100	Defines density (64M/72M)
JEDEC Code (11:1)	000 0011 0010	Unique identification of SRAM vendor (32 hex for Enhanced Memory Systems)
ID Register Presence (0)	1	Indicates the presence of an ID register

Scan Register Sizes

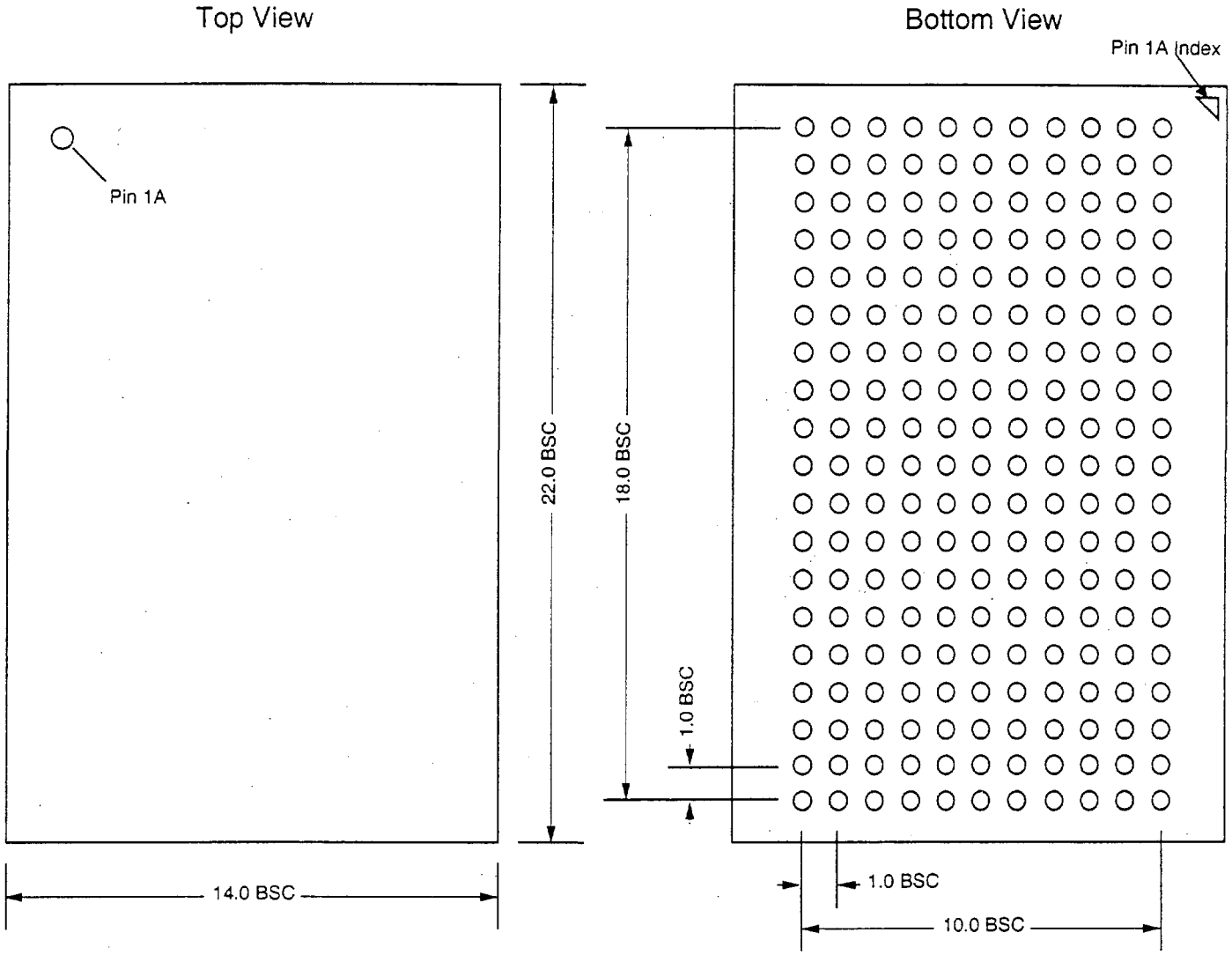
Register Name	Bit Size
Instruction	3
Bypass	1
ID	32
Boundary Scan	67

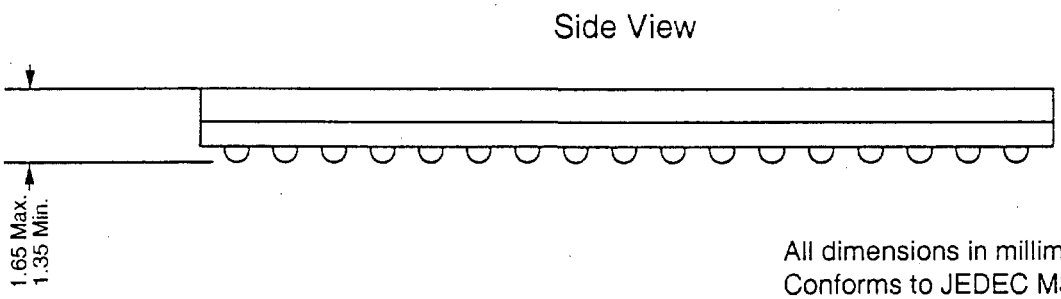
Instruction Codes

Instruction	Code	Description
EXTEST	000	Captures the input/output states. Places the Boundary Scan register between TDI and TDO. Forces all outputs to high-Z state. This instruction is not 1149.1 compliant.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect device operation.
SAMPLE Z	010	Captures the input/output states. Places the Boundary Scan register between TDI and TDO. Forces all output drivers to a high-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures the input/output states. Places the Boundary Scan register between TDI and TDO. Does not affect device operation. This instruction does not implement the 1149.1 preload function and is therefore not 1149.1 compliant.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the Bypass register between TDI and TDO. Does not affect device operation.

Mechanical Drawings

Package Dimensions (209-ball PBGA)





All dimensions in millimeters
Conforms to JEDEC MS-028C, variation BC
Drawings are not to scale

Revision Log

Revision	Date	Summary of Changes
0.81	9/21/00	Changed ZQ pin location.
0.9	12/21/00	Changed pin assignments, added JTAG description, changed initialization sequence.
0.91	1/5/00	Revised Deselect description. Updated CK/CK# input capacitance.
0.92	3/28/01	Updated Power Supply Standby current. Updated CK/CK# input capacitance. Removed "DO NOT COPY" restriction.
0.93	5/18/01	Revised Deselect command description and changed t_{REF} min/max values. Changed read timing diagrams to show extended data phase on 8th read bit. Changed I_{OH}/I_{OL} min/max values. Changed t_{CQD} min/max values. Changed Power-Up Sequence. Clarified portions of JTAG descriptions. Updated mechanical drawings.
0.94	7/25/01	Removed requirement that controller must hi-Z data bus at power-up. Added Boundary Scan Order table. Added 'E' to part numbers. Added "subject to change" note to package height.
0.95	6/18/02	Changed t_{CQD} timing spec, added t_{AH} timing spec, changed I_{DD} and I_{SB}, fixed package height.
1.0	11/26/02	Redefined –3.3 and –4 speed grades as –3.0 and –3.6. Added –4.5 speed grade. Changed alternate bank write to read command spacing to 6 cycles. Changed I_{DD} and I_{SB} values. Added clock high level parameter V_{CKH}.

Ordering Information

Part Number	R/W Latencies	I/O Width	I/O Type	Package	Power Supply	Clock Frequency (MHz)
SS2615B-3.0E	4, 6	x36	1.2V HSTL	209-ball PBGA	2.5V	333
SS2615B-3.6E	4, 6	x36	1.2V HSTL	209-ball PBGA	2.5V	278
SS2615B-4.5E	4, 6	x36	1.2V HSTL	209-ball PBGA	2.5V	220

Exhibit R – Part 2

Pegasus Design Target

1. PURPOSE

This Data Sheet Addendum together with the HP SS2615 Data Sheet, Revision 1.0, constitutes the full specification for the 2Mx36 DDR ESRAM to be manufactured by Enhanced Memory Systems for Hewlett Packard. These Addendum specifications take precedence over those in the Data Sheet.

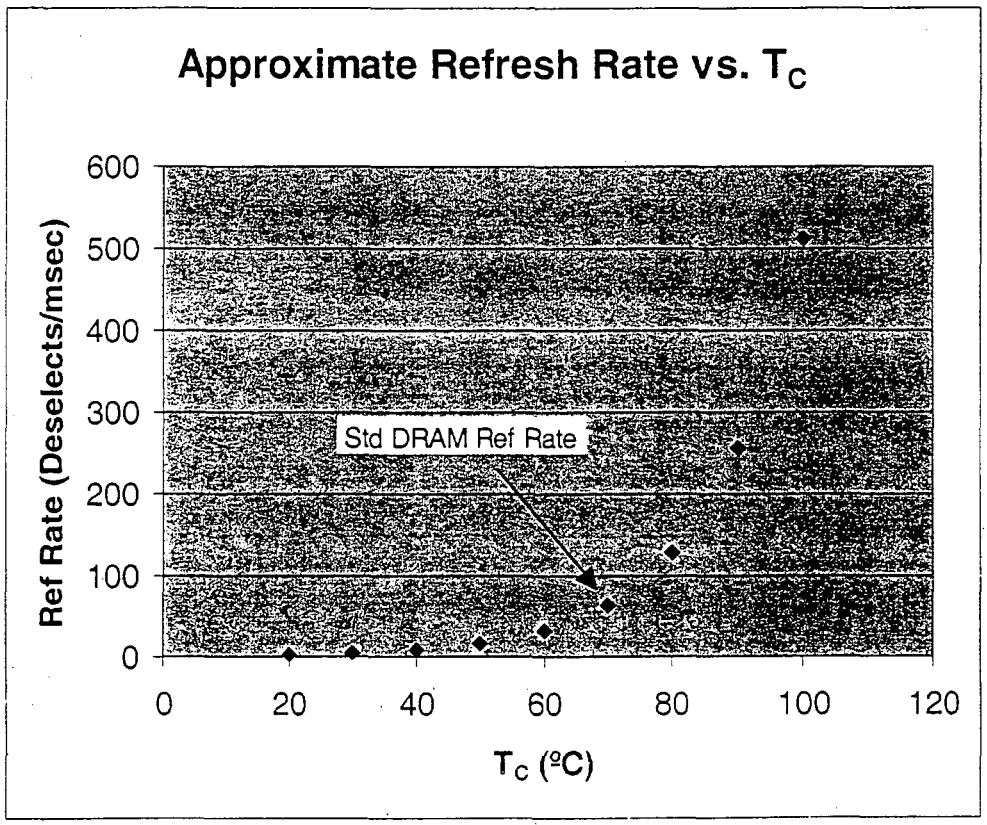
2. APPLICABLE DOCUMENTS

The -3.6 Speed Grade columns on the Data Sheet should be referenced as the specification to be developed by Enhanced Memory Systems for delivery to Hewlett Packard. If devices specified to other Data Sheet speed grades are provided to Hewlett Packard by Enhanced Memory Systems, those devices must also meet all provisions of the Data Sheet, Addendum, and Manufacturing Contract.

3. FUNCTIONAL ATTRIBUTES

3.1. Refresh Operation

3.1.1. Refresh requirement is not frequency dependent, however it is temperature dependent.



4. AC & DC CHARACTERISTICS

4.1. V_{DD}/V_{DDQ} Current Specifications

4.1.1. I_{DDQ} (max), is expected to be 120 mA with no output load.

4.1.2. I_{DDQ} (max), is expected to be 370 mA with a 20pF load.

4.1.3. I_{DD} (max) is 550mA for –3.6 devices operating at a frequency of 200MHz.

4.2. ZQ Resistor Value, Z_0 Limits

4.2.1. Z_0 target range is 25 to 55 ohms, which allows an RQ range of 125 to 275 ohms.

4.3. Power Supply AC Limits

4.3.1. V_{DD} AC Specification: At the package pins, V_{DD} AC noise can be ± 100mV (200mV p-p) max at frequencies > 100MHz relative to the DC value measured at < 100MHz. The device will present to the power supply an AC load of 50mA/ns (max).

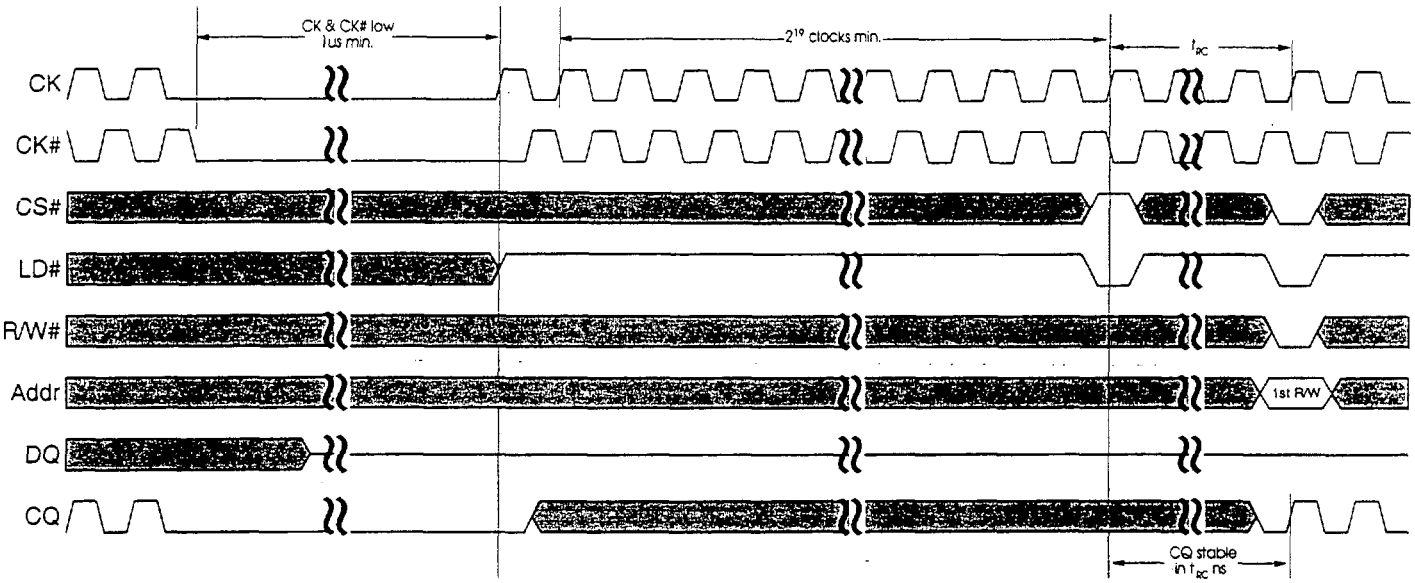
4.4. Input Clocks Specification for Soft Reset Operation

4.4.1. The device employs a soft reset feature that internally resets the refresh counter and other logic circuits. This feature allows the memory to restart to a known state without the need to cycle power supplies. The soft reset state is entered when both CK and CK# inputs satisfy the V_{IL}(max) specification shown below. Soft reset will not interfere with the JTAG operation.

Symbol	Parameter	Min	Max	Units
V_{IL}	Input Low Voltage for CK, CK#	-0.3	V_{ref} – 0.3	V

4.4.2. The input clocks CK and CK# must comply with the following, rather than what is specified in the data sheet, when $V_{REF} \leq 0.6V$: V_{CKH} (min) = V_{REF} + 0.03V.

4.4.3. Soft Reset Timing



Notes:
1. During soft reset, no metastable inputs are allowed on LD#, CS#, R/W#, or address pins.
2. The maximum time both input clocks (CK, CK#) may be low without entering soft reset is 7ns.

4.5. DQ Output Enable/Disable Timing

4.5.1. We guarantee by design not to drive to the opposite data state and then hi-Z.

4.5.2. Output disable monotonicity will be guaranteed by design. HP agreed to drop the requirement for monotonic enabling.

4.6. DQ Output Rise/Fall Times

4.6.1. Parameters t_R and t_F, referenced in the data sheet, are not tested but rather characterized and guaranteed by design within the maximum input rise/fall times as specified.

4.7. Additional Input Specifications

4.7.1. The maximum differential rise and fall times of CK/CK# will be 0.5ns, measured at 20% to 80% of VDF (min).

4.7.2. The maximum rise and fall times for address, control, and data inputs will be 0.4ns to 0.6ns, measured at V_{IH} (min) and V_{IL} (max).

t_{TCK}	t_T max.
0.1 ns	0.4 ns
0.2 ns	0.4 ns
0.3 ns	0.5 ns
0.4 ns	0.6 ns
0.5 ns	0.6 ns

4.7.3. AC specifications are guaranteed by design and characterization over this rise and fall time range.

4.7.4. In order to maintain the guarantee of correct DRAM operation, it is sufficient that the system-generated AC waveforms, measured at the DRAM input balls, meet the AC timing parameters, VIH and VIL specifications, and rise/fall time specifications listed in the data sheet and HP addendum. A suitable method to be used to guarantee that the DRAM devices simultaneously meet all of these specifications has not yet been developed, however it is agreed that simulation and characterization results are not, by themselves, sufficient. It is also agreed that direct production testing at guard-banded worst-case conditions may not be possible. It will be the responsibility of EMS to develop a testing methodology sufficient to reasonably ensure that these criteria are met.

4.7.5. CK and CK# input signals must be monotonic on a single-ended basis only while the differential voltage is within the □ 0.4V window.

4.7.6. Input arrival time is greatly affected by the DRAM capacitive input loading as compared to the rise times and setup and hold times. Because of this effect and because we can only measure input arrival time at some distance up the board trace from the DRAM solder ball, the direct scope measurement we must rely on is that of the input waveform edge reflected off the die back to the probe point. Input arrival time at the DRAM pin for all input specs shall be defined as the arrival time calculated at the die pad from such a measurement minus the small speed-of-light delay calculated for the package trace from the DRAM solder ball to that particular DRAM die pad.

4.8. VDDQ Noise Reduction

4.8.1. On-chip decoupling of V_{DDQ} is implemented as > 2 nF per DQ pad with a series resistance target of < 2 ohms.

5. PACKAGE DESIGN

5.1. Package Trace Lengths

Signal	Min.	Max.	Units
CS#, LD#, R/W#	5.0	8.8	mm
A, BA	4.5	10.9	mm
CK, CK#	4.10	4.15	mm
CQ, CQ#	3.35	3.53	mm
DQ	3.0	6.2	mm

5.2. Package Trace Impedance

5.2.1. Package trace impedance target is 65 ohms and the target range is ± 10%. Package vendor will characterize.

5.3. Pin Assignment

5.3.1. Although pin location 8R is labeled Vss in the SS2615 data sheet, it is a normally high-Z test signal and is not connected to the Vss package plane. However, this pin will not

adversely affect device operation if it is connected to Vss. It is used only for diagnostic purposes.

Exhibit S

ORDERING AND PAYMENT TERMS FOR CONTRACT ENGINEERING SERVICES

1. Contract Engineering Services. EMS and/or RIC will provide those contract engineering services described in Section 7 of this Amendment and as further described in the attached Exhibit F-2, above, on a full-time basis, subject to and in compliance with the terms and conditions of this Agreement and all applicable laws. All contract engineering services will be performed at the request of HP, and are more specifically described in, and authorized by, a Purchase Order and the Statement of Work set forth in Exhibit R. The terms and conditions of this Agreement will apply to all such Statements of Work.

2. Basis of Compensation. EMS and/or RIC will be paid for contract engineering services and be reimbursed for expenses according to the Direct Personnel Costs specified in Section 11 of this Amendment. No proposed change in the Direct Personnel Costs will be effective unless approved in writing by HP.

3. Invoices. EMS and/or RIC will invoice HP monthly unless otherwise expressly stated in the Purchase Order. With each invoice, EMS and/or RIC will submit supporting documentation in a form satisfactory to HP and in detail sufficient for HP to identify the contract engineering services rendered and the costs and expenses incurred in the performance of the contract engineering services. HP may deduct from EMS' and/or RIC's outstanding invoices any monies owed to HP by EMS and/or RIC.

4. Payment by HP. HP will pay the undisputed amount due EMS and/or RIC within forty-five (45) days from the date of receipt of the invoice and any documentation required under this Agreement. If any amount claimed by EMS and/or RIC in any invoice is disputed by HP, the parties will negotiate in good faith to resolve the dispute. EMS' and/or RIC's acceptance of payment will constitute a waiver of any claims of EMS and/or RIC for payment for contract engineering services covered by the disputed invoice.

5. Maximum Cost. The "Maximum Cost" to be paid to EMS and/or RIC for contract engineering services will be the amount authorized in applicable Purchase Orders authorizing the contract engineering services. EMS and/or RIC will not perform contract engineering services in excess of the Maximum Cost specified in the Purchase Order unless authorized in advance by HP in a Change Order.

6. Most Favored Pricing. EMS and/or RIC warrant that the prices charged for the contract engineering services are not in excess of the lowest prices charged by EMS and/or RIC to other similarly situated customers for similar contract engineering services .

7. Taxes. EMS and/or RIC will have sole responsibility for the payment of all employee taxes, compensation, wages, benefits, contributions, insurance, and like expenses, if any, of its employees. EMS and/or RIC will indemnify and hold harmless HP, its officers, directors and employees from and against all liability and loss in connection with, and will assume responsibility for payment of, all federal, state and local taxes or contributions imposed as required under employment insurance, social security and income tax laws for EMS' and/or RIC's employees engaged in the performance of this Agreement.

8. VAT Taxes.

8.1 All prices mentioned in this Agreement are inclusive of any value added taxes, or other similar taxes, (including but not limited to Canadian goods and services tax) ("GST"), Japanese consumption tax ("JCT"), and the like (individually and collectively, "VAT").

8.2 Where applicable, EMS and/or RIC will ensure that its invoices to HP or its Affiliates (collectively "HP") meet the requirements for deduction of input VAT by HP.

8.3 All prices mentioned in this Agreement are exclusive of any US sales or use tax.

8.4 All payments made by HP under this Agreement may be reduced by the amount of any applicable foreign government withholding tax, provided that HP provides the related documentation to EMS and/or RIC, including tax receipts and any other documentation necessary and appropriate to establish that all such taxes have been paid and are available to EMS and/or RIC for credit for United States income tax purposes. EMS and/or RIC and its subsidiaries will be jointly and severally liable for, and will bear the full economic burden of any such taxes.

8.5 HP will cooperate with EMS and/or RIC in applying for any tax reduction permitted under any such foreign government law.

8.6 If there are specific legal requirements within a given legal jurisdiction regarding the contents of this Agreement, a purchase order or an invoice, the parties agree to make any and all changes required by such legal jurisdiction.

8.7 HP will not be responsible for the payment of any duties or taxes imposed on the income or profits of the EMS and/or RIC.